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S-51 REAL TIME DATA REDUCTION SYSTEM

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SUMMARY

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The S-51 Real Time Data Reduction System decommutates and recognizes an analog and digital pulsed frequency modulated telemetry format of 16 channels per frame at a rate of 50 channels per second. For the digital input of three bits per channel, the system recognizes eight discrete frequency bands between 5KC and 15KC and converts these frequencies to a decimal number and prints the number and its identification on a paper tape. For the analog input the system prints the 10-period average. This report contains a description of the telemetry format, the system components, the type of logic used, and the operation of the system.

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II S-Pac Digital Modules Instruction Book.
Computer Control Corporation

III Hewlett-Packard Electronic Counter 523/CR Instruction Book

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S-51 REAL TIME DATA REDUCTION SYSTEM

INTRODUCTION

PURPOSE

The design and construction of special-purpose equipment was undertaken in order to facilitate "real time" data reduction for the UK-1(S-51) satellite program. This has resulted in a system which separates, collates, and displays both the analog and digital information, in decimal form, on a printed paper tape. The speed and clarity in data readout from this system are such as to warrant its use for "quick look" data reduction in the evaluation of the satellite telemetering performance while it is on the test stand or in orbit.

DESCRIPTION OF TELEMETRY FORMAT

A complete description of the telemetry format is presented in the reports entitled "UK-1(S-51) Encoder," and "Proposed Requirements for Satellite S-51 Test Stand Telemeter Data Reduction System". Presented here will be only that part of the format which is considered necessary to the understanding and operation of this system.

There are two types of transmitted data groups which will be referred to as the "high speed sequence" and the "low speed sequence". The demodulated input to the data reduction system will be a series of pulses in the frequency range from 4.5KC to 15.4KC. The pulse durations are 10ms with 10ms intervals, except for the frame sync. pulses which are of a 15ms duration preceded by a 5ms interval. Each pulse (burst) with its preceding interval (blank) is referred to as a channel. Sixteen channels comprise a frame. Channel "0" of every frame is reserved for frame sync and identification. All the remaining channels are either digital data channels or analog data channels. Refer to tables #1 and #2 in the report, "UK-1(S-51) Encoder" for channel allocations. Information is conveyed in terms of the frequency within the burst of these channels. The analog channels will contain a variable frequency, while the digital channels will contain, at any given time, one of eight possible discrete frequencies. Each discrete frequency represents a binary number in octal form.

The digital data channels are used for the Cosmic Ray and X-Ray experiments. The designation for the number contained in a channel will be one of the following: C_1, C_2, C_3, C_4, C_5, C_6, X_1, X_2, X_3, X_4, or X_5.

The basic difference in the signal format for the high speed and low speed sequence is that the high speed sequence is composed of 16 frames, while the low speed sequence is composed of 2 frames. The other distinguishing feature of the low speed sequence is that

the normally blank periods now consist of a stable 15.4KC calibrating signal. Another feature worth mentioning at this point is the channel "0" burst frequency of 4.5KC which is present in every other frame during the high speed sequence, and in frame "0" during the low speed sequence. The 4.5KC, 15.4KC, and 5KC detected envelopes serve important logic functions in the data reduction, as will be described later.

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GENERAL DESCRIPTION

The system is composed of eleven main units, cabled together in one double six foot rack, as follows:

DECOMMUTATOR This unit serves to process the demodulated signal and separate the various channels of information. It is completely described in Appendix I.

COMB FILTER This unit is composed of ten modular filter boards, a matrix board, a board consisting of eight inverter amplifiers, and a power supply board. Eight of the filter boards are used for converting the digital data from the octal to a binary representation. The other two filters present an output for identifying the 4.5KC and 15.4KC synchronizing frequencies.

CONTROL SYSTEM The logic has been designed employing the Computer Control Company's 1 megacycle series S-pacs, which are based on the Nand logic circuit. A description of these transistorized modules and their application is provided in the instruction manual, Appendix II.

The packaging of the S-Pac modules has resulted in three groups of 28 connectors. Each group is referred to as an S-Bloc. The designation for any given wire location, on the drawings or referred to in the logic description, will be a group of three numbers. These numbers will identify the S-Bloc, the S-Pac, and the connector pin in that order. For example, the number I-3-27 refers to S-Bloc number I, S-Pac number 3, and pin number 27 on the connector.

There are a total of 71 modules employed in the logic which are distributed with 28 on S-Bloc I, 25 on S-Bloc II, and 18 on S-Bloc III. Two of the modules are special purpose circuits which were adapted for use on the S-Pac type of printed circuit board. They are the gated oscillator and the 320 cycle per second filter.

POWER SUPPLY The Computer Control Company's regulated 8 ampere, model RP-31 supply is employed for operation of the logic modules. Each other unit in the system has a built in DC power supply.

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CONTROL BOX This consists of a front and back control panel serving as the control center for wiring distribution and operating mode selection. The "channel ID" voltage divider, "signal sensor", and "buffer amplifier" circuits are located on terminal boards in the control box.

DIGITAL CHANNEL DATA PRESENTATION This encompasses the modified Hewlett-Packard 523CR counter, 560-A printer, and special-purpose decades (4G and 4E). The counter was modified such that the sixth and most significant stage is operated independently from the first five cascaded stages. This stage displays the sensitivity bit as a 0 or 1, while the digital number read-out is displayed by the first five stages which are operated in the time interval mode of counter operation.

The special purpose decades referred to are the four type 4-G decades which are cascaded to form the "Sequence Counter" and the single type 4-E decade employed as the "Dig.No. Flag". These decades are driven and reset from transistor amplifier circuits mounted at the rear of the same chassis.

The 560-A printer has an eleven column capacity. The print wheel staircase voltage control for the first six columns emanates from the 523CR counter in the normal manner. Staircase voltages to the remaining five print wheels are generated by the decades and introduced to the print wheel voltage comparators through an added cable. The digital channel print-out representation, reading from right to left, is as follows:

The first five digits display the "Decimal Number".
The sixth digit displays the "Sensitivity Bit".
The seventh digit displays the digital number identifier, "Dig. No. Flag."
The eighth through eleventh digits display the "Sequence Count".

ANALOG CHANNEL DATA PRESENTATION A Hewlett-Packard 523CR counter, 560-A printer, 4-G decades, and a precision resistor voltage divider are used for this presentation. The counter is not modified but functions only as a four-stage, ten-period-average counter. Four decades are cascaded to operate as a sequence counter. These are driven and reset by transistor amplifiers mounted on the rear of the same chassis. A voltage divider, mounted on a terminal board in the control box, controls two print wheels. The voltage to these wheels is selected by the channel selector switch on the control panel, such that the print-out will be a number 0 through 15. This identifies the channel being processed.

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The printer receives the staircase voltages from the period counter, sequence counter decades, and a d.c. voltage from the Channel ID divider such that the print-out column identification, reading from right to left is as follows:

The first four digits display the ten period average.
The fifth digit remains on the character to which it is manually preset, preferably a zero or blank.
The sixth and seventh digits display the channel ID.
The eighth through eleventh digits display the sequence count.

LOGIC DESCRIPTION

A. Input Selector

Refer to figures 2, 3, 4 and 23.

The "input selector" encompasses the logic and circuitry required to insure a proper input to the "Decommutator Proper", which is referred to as board #2 input. Normally, this input originates from the "Decommutator front-end", or board #1. In this case, however, the "burst-blank envelope" input to board #2 is "gated" from board #1, through a buffer amplifier, during the high speed sequence data, and from the 15.4KC comb filter during the low speed sequence. This separation was necessary because the Decommutator front-end was not designed to process signals having the C.W. characteristic of the low speed sequence data, resulting from the 15.4KC signal present during the normally blank periods.

The demodulated signal input from the receiver or tape deck is selected by a switch on the control panel and then parallel fed to the signal sensor and decommutator board #1 input.

1. Input signal sensor (located on terminal board in control box). This circuitry, Figure 3, was incorporated to prevent the Decommutator from being triggered by extraneous noise during the periods of no signal input. Emitter follower Q-1 is biased to conduct only during signal amplitudes of 0.5 volts or greater. Amplifiers Q-2 and Q-3 serve as a signal level detector. The collector of Q-2 and base of Q-3 will be at ground level during the burst or conduction periods of Q-1 and will be held at this level, during blank periods, for as long as 50 milliseconds by the large capacitance at the collector and base,respectively. The collector of Q-3, therefore, will be at a -6 volt level when data signals of 0.5 volts or greater are present at the input to the Decommutator.

2. Buffer amplifier Figure 4 (located on terminal board with Input Signal Sensor). The detected burst-blank envelope output from board #1 of the Decommutator, during high speed data processing, is "buffered" by these two amplifier stages to prevent loading of the emitter follower Q-12. The signal is then fed to one input of a three input "nand gate", II-16-22, and the inverted output at III-2-9 is again inverted by the "nor gate" at III-2-6. This presents a burst-blank envelope, which is negative during burst time,to drive input board #2 of the Decommutator.

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3. High speed-low speed selector -- Automatic switching is required to control the characteristically different inputs to the Decommutator proper whenever the signal changes from either high or low speed data. This switching is accomplished electronically by use of a bistable multivibrator or "flip-flop" having outputs at II-10-6 and II-10-23. During low speed data operation, there will be continual positive going pulses at II-10-19, from the 15.4KC comb filter inverter II-10-33, and no inputs at II-10-26. This will serve to hold output II-10-6 at -6 volts and thereby gate the 15.4KC envelope through to II-16-34. A positive pulse will occur at II-16-14 which signifies the end of the low speed data transmission and "flips" the multivibrator, resulting in a negative state at II-10-23. A positive trigger will also occur during channel (0) of every other frame, resulting from the 4.5KC comb filter output, in the high speed mode of operation. This control pulse is introduced at II-18-11 and serves to insure that the "flip-flop" remains in the state which gates the high speed data burst-blank envelope out at II-16-27. The "nand gate" input, II-18-13, will remain at the -6 volt level during the high speed mode, resulting in a positive output pulse at II-18-16 for every negative input at II-18-11. A 15 microsecond delay is introduced at the DM output II-24-29 by triggering from the trailing edge of the output pulse from the DM at II-24-31.

4. Eliminate 4.5KC output on L.S. ---- The 4.5KC frequency is contained in the burst of F(0) C(0) on low speed data and, therefore, presents an enabling pulse to the nand gate at II-18-11. This gate is inhibited during low speed processing to prevent the pulse from falsely triggering the selector "flip-flop" into its high speed state. To accomplish this, II-18-13 is held at ground. See timing diagram Figure 23.

5. Sync pulse shaper -- This logic circuitry was designed to insure that the burst envelope input to board #2 of the Decommutator for every channel (0) shall be a minimum of 14 milliseconds wide. The gate at III-9-12 is enabled only during the channel (0) burst time due to the 6 milliseconds of delay, at III-9-17, from the leading edge of the 5 millisecond blank. Output III-11-31 therefore can occur only once per frame, and is adjusted for a 14 millisecond width.

6. Flywheel -- The input to the astable multivibrator at III-15-26 is the burst-blank envelope. When this input is at the logical one state (-6 volts) the multivibrator will free-run and generate 10 millisecond pulses at the output pins 17 and 35.

During periods of missing bursts, the start input III-15-26 will remain at the -6 volt level, the multivibrator will free-run, and there will be no interruption of the 10 millisecond pulse outputs. These pulses are fed into the Decommutator counter and strobe generator to avoid losing synchronization.

B. Strobe Generator, L.S. Frame Sorter, and L.S. Programmer. Figures 5 and 24.

1. Strobe generator - A 9.4 microsecond "strobe" pulse is generated at DM I-22 output pins 10 and 29 which is delayed by 6 milliseconds from the start of each channel burst appearing at I-22-25. Each delayed strobe is then "anded", through an individual "gate", with its synchronized burst envelope from the Decommutator. The result is a time marker pulse output to identify the approximate mid-point of any channel burst time employed in this system. Generation of a channel (0) strobe is described with timing diagrams in Figure 24.

2. L.S. Frame Sorter - Each low speed sequence is composed of two frames, referred to as frame (0) and frame (1). There is a requirement, therefore, to identify each frame at the proper time. The 4.5KC comb filter presents an output at each F(0) C(0) which is used for a time reference. This 4.5KC envelope is amplified, inverted, and enables an "and gate" at II-5-20, Figure 5. The low speed F(0) C(0) strobe output at II-5-34 triggers the set input of U.F. II-9-24. The set output II-9-26 will then be in its negative state until reset at the end of channel 15 and will be referred to as the F(0) bracket. Delay multivibrator II-8 receives a positive trigger at its input pin 25 when the reset occurs at II-9-26. It, in turn, generates a 10 microsecond trigger to "flip" II-9-15 to its negative state which will represent the F (1) bracket.

3. L.S. Programmer - A group of ten 2-input nand gates are shown in Figure 5. Each gate is enabled by a specific frame bracket at one input and a channel strobe at the other, resulting in an output strobe pulse to represent this time in the logic. For example, during F(0) C(8) time there will be an output strobe pulse at I-15-23. This is due to the fact that the "nand" input I-15-30 is at a -6 volts when the negative strobe representing channel (8) appears at I-15-26. The above example is illustrated by the timing diagrams of Figure 24.

C. H.S. Frame Sorter, Corrector, and Programmer. (Figures 6, 7, and 26)

1. H.S. Frame Sorter - A high speed sequence consists of 16 frames of information requiring separation and identification

for performance of logic control. The method employed, as shown in Figure 6, is to count the frames in a scale of 16 binary counter, load this count into a matrix, which, in turn, controls the outputs of a group of "nand gates." Each "nand gate" positive output will last for a period of one complete frame and is referred to as a frame bracket. An output is determined by a negative state at all four inputs to any given "nand gate", which can logically occur only once per sequence. The count is properly synchronized by presentation of a reset pulse, from the 5KC comb filter, to BC II-11-19 during each F(0) C(0) time. It should be noted that the frame count input at II-11-22 is delayed for 5 microseconds by DM II-12-31 in order to avoid a "race" with the reset pulse occurring simultaneously.

The output of the "nor gate" I-28-6 presents a marker pulse, through a back panel BNC jack, to operate a strip chart recorder. The gate is enabled at I-28-18 with the burst envelope selected by the "channel selector" switch (10-B) located on the front control panel, and at I-28-19 by a 5 millisecond pulse during F(0) C(0) time for high speed or low speed data. The strip chart will, therefore, record the beginning of each sequence and the position on the graph of the selected information channel.

2. H.S. Frame Corrector - The loss of one or more frame counts is possible, due to loss of synchronization or signal fading. In order to avoid the loss of data for an entire sequence, the frame counter receives correction pulses during every other frame. These pulses are applied to the set and reset nodes of the counter in such a manner as to realign each stage to the proper state when the loaded count doesn't agree with the frame corrector count. The correct frame number is readily determined at the comb filter matrix output. This binary output is processed through the "and" matrix III-4, which presents an output, representing the decimal number, to enable one of seven "nand" gates at any given time. The common inputs to these gates, shown in figure 6, are enabled by the channel (0) strobe. For example, there will be an output pulse at III-3-34 only during F(2) C(0) which will appear at II-11-21, II-11-30, II-11-13, and II-11-8 insuring that the counter is in the proper state for a count of 2.

3. H.S. Programmer - (Figure 7) A group of eleven "nand gates" are employed to program the H.S. control timing pulses for logic functions in the system. Each gate is enabled at one input by a strobe pulse representing either channel 1, 2, or 3 and at the other input by a specific frame bracket. The gated outputs will, therefore, be strobe pulses, each representing a

different channel of information within the telemetered data format. For example, the strobe output at I-20-16 will occur only once per sequence during F(14) C(2) and is used to enable one input (I-4-22) of a register loading control gate. The function performed at this time may be readily seen by reference to the control timing chart, Figure 21.

The reset pulse to the digital number flag decade is produced at the "nor gate" output I-12-7. This occurs once during each low speed sequence F(0) C(8) input at I-12-14 and once during each high speed sequence F(1) C(0) input at I-12-9. A pulse used to reset the register is developed at the four-input "nor gate" I-14-9. The input control pulses to this gate are at I-14-6 during high speed F(0,8) C(0); I-14-7 during low speed F(0) C(3); I-14-23 during high speed F(14) C(0) and I-14-24 at the end of the high speed data transmission.

The original design of this equipment included "nor gates" having outputs at I-18-17 and I-18-21 representing the print command pulse to the digital printer and the reset pulse to the decimal counter, respectively. The method of programming the decimal counter and printer has since been changed in order to simplify the modifications to the Hewlett-Packard counter; consequently, although still connected in the logic circuitry, the two "nor gates" are not being employed.

D. End of High or Low Sequences. Figures 10, 27, and 11.

The end of transmission of high speed or low speed telemetered data is preceded by a signal as described in the data format. A method of detecting and processing these signals was required in order to develop a control pulse for resetting the sequence counters to zero before the start of each new transmission. This pulse is also employed in the register logic at III-5-9 to start the decimal counter for a zero print-out. The H.S.-L.S. selector "flip-flop" is set to the high speed state at the end of low speed transmission by enabling the "nor gate" at II-16-14.

1. End of high speed sequence - The two second transmission of the 320 cycles per second signal, which signifies the end of high speed data, is detected by an RC active filter employing regenerative feedback, Figure 11. The input emitter follower, Q-1, constitutes a high pass filter stage which is followed by a single stage low pass filter, Q-2. A bandpass of approximately 270 to 700 cps is achieved by the two stages. The signal is then detected at the collector of Q-3 which drives the saturating

amplifier Q-4. The end of high speed data is, therefore, indicated by a negative output at the collector of Q-4 for a period of two seconds. The "nor gate" output III-13-27 is inhibited for a period of one second by DM output III-14-31 to prevent filter output transients from resetting the sequence counters. A filter output duration of greater than one second is considered legitimate and results in a 2.5 millisecond positive pulse output at III-13-6. See timing diagram, Figure 27.

2. End of low speed sequence - The output of II-16-23 will be a 200 microsecond positive pulse which can only occur when the negative input at II-16-30 has a duration of greater than 15 milliseconds, as is normally the case for the 40 millisecond period of 15.4KC transmission at the end of the low speed data. The pulse timing at II-16-26 is controlled by two time sharing delay multivibrators having outputs at II-17-29 and II-20-29, which are controlled by the state of "flip-flop" UF II-22 and the start of each blank of the burst-blank envelope appearing at II-16-17. The resulting output at II-16-6 is a negative 15 millisecond pulse, starting at the beginning of each blank (15.4KC envelope). The trailing edge of this pulse will trigger DM II-17-6 to produce a negative output which, when occuring simultaneously with the negative period of input II-16-30, will enable the "nand gate". Refer to timing diagram, Figure 27.

3. Decimal counter control - The "nor gate" output at II-21-2 is used to reset and start the decimal counter. A 200 microsecond pulse is then produced at II-17-28 and II-21-27 to stop the counter which, in turn, commands a print-out from the digital recorder. This print-out of zeros, therefore, signifies the end of either a high or low speed sequence.

A stop pulse is normally presented to the decimal counter at the end of each decimal number. This same pulse from inverter output II-21-7 is used to trigger the delay multivibrator input II-20-9. The DM output II-20-28 inhibits the "nand gate" at input II-21-13, while the output from II-20-17 enables the "nand gate" at input II-21-26 for a period of 200 milliseconds. During this period, an end of sequence pulse appearing at "nor gate" output II-19-9 would enable only the "nand gate" having its output at II-21-23. A 200 microsecond positive pulse, delayed for 300 milliseconds, will then be generated at the DM.output II-8-28. This delay introduced to the "end of sequence" control pulse is necessary to avoid disturbing the print wheel positions while the printer is engaged in a print cycle following a decimal counter stop command.

E. Sequence Counter Control and Digital Number Identifier (Figures 9 and 25)

1. Sequence Counter Control - The digital channel sequence counter receives count pulses from the "nor gate" output II-19-21 while the analog channel sequence counter receives counts from inverter output III-19-6. Both counters, however, will advance one count for each "sequence". The added circuitry for the analog counter control was required to prevent undesirable repositioning of the print wheels during the print cycle of the recorder. Since the print command pulse to the analog recorder can occur during any one of the sixteen channel periods, dependent upon the channel switch selection, it is impossible to have a fixed time for recording the sequence counts and allow the required 200 milliseconds for a complete print-out cycle. Therefore, the sequence count is "stored" by setting the UF output, II-22-15, to its negative state. When the selected burst envelope appears at inverter output III-19-16, the sequence count is "gated" out at III-19-12, inverted at III-19-6, and presented to the input amplifier which drives the counter. The positive going trailing edge of the burst envelope at III-19-16 resets UF output II-22-15 to its positive state. The sequence counts for high speed data are introduced at "nand gate" input III-19-21, whereas the low speed sequence counts are introduced at III-19-25. The 300 millisecond DM output pulse at III-8-29 triggers the UF input II-22-17 and inhibits the "nand gate" at input III-19-29 to insure against extraneous counts for the duration of the frame.

The low speed sequence count to the digital channel is presented at the "nor gate" input II-19-20 during F(0) C(8) which was selected as the most advantageous time. This selection was possible since the digital channel printer receives each print command at a fixed time from the control logic.

The high speed sequence count to both counters is normally introduced at II-19-18 during F(0) C(0). A missing burst during this time would, therefore, result in the loss of a proper sequence count. Logic circuitry is employed to correct his situation by presenting a count pulse at II-19-19, during F(8) C(0), only if the normal count pulse was not present at II-18-31. This is controlled by the "flip-flop" composed of two "nand gates" having outputs at II-18-34 and II-18-33. The appropriate outputs, occurring only during frame 12 from the frame counter of the simulator, are "anded" to give a positive output at II-19-17 having a duration of 320 milliseconds. This pulse inhibits the gate at II-18-21, resulting in the negative or reset state for the output at II-18-34. It then requires a positive trigger at the

set input, II-18-31, of the "flip-flop" to return II-18-34 to ground or logical zero. When this normal set trigger occurs during F(0) C(0), the "nand gate" input at II-19-11 will be at ground until reset again by the frame 12 bracket pulse. The "nand gate" is, therefore, inhibited during this period. However, should the set pulse not be present, the output at II-18-34 would remain in its negative state, thereby enabling the gate at II-19-13. This would occur during F(8) C(0) and result in a positive strobe pulse output due to the enabling inputs at II-19-10 and II-19-12. These inputs represent the channel 0 strobe pulse and the outputs, representing the binary number four from the comb filter, respectively. A positive output pulse at II-19-13, therefore, constitutes a correction for a missing high speed sequence count.

The channel and frame counters employed in the simulator receive a reset pulse through switch 1 (E-2) when in the operate position. This occurs during F(0) C(0) and insures that the channel and frame output pulse representations will be nearly synchronized with the input signal. A difference in the 50 cps clock rate resulting in an error of $\pm$ four frames per sequence can be tolerated.

2. Digital number identifier - This consists of a "nor gate" having five inputs at II-15-8 and an output at II-15-9 which drives the decade counter referred to as the "Dig. No. Flag". This decade controls a print wheel in the digital channel printer which identifies the decimal number being printed. During a high speed sequence, each print out will present a number between 1 and 5 as follows:

(a) Identifying C_1 through C_4 accumulated data during f(1) C(1).
(b) Identifying C_5 and C_6 accumulated data during f(2) C(1).
(c) Identifying C_1 through C_4 accumulated data during f(9) C(1).
(d) Identifying C_5 and C_6 accumulated data during f(10) C(1).
(e) Identifying X_1 through X_5 accumulated data during f(15) C(3).

During a low speed sequence, each print out will present a number 1 or 2 as follows:

(a) Identifying C_1 through C_4 accumulated data during f(0) C(11).
(b) Identifying C_5 and C_6 accumulated data during f(1) C(9).

F. Register -- Refer to Figures 8, 28, and 30.

1. Storage and input multipliers.

The binary representation of the digital data is stored in a fifteen stage binary counter composed of cascaded BC boards I-2, I-3, I-6, and I-7. The DC set input of each stage is loaded or controlled from the output of an individual "nand gate" which serves to gate through one bit of the binary output from the comb filter during the prescribed times in each sequence. Three stages of the binary counter are required for storing the octal representation of the data contained in each digital channel (after conversion to binary form). The three-stage groupings within the register are loaded with digital data as follows:

Group	Digital Number
1	C_1 or C_5 or X_1
2	C_2 or C_6 or X_2
3	C_3 or X_3
4	C_4 or X_4
5	X_5

Loading and readout timing are presented on the register logic drawing, Figure 8, and the control timing chart, figure 21.

The method employed in converting the comb filter binary output number to decimal form is to load the register with the bit by bit complement of the number, add one count, and then determine how many more counts (N) are required to reset the register to zero. The number(N) is then the decimal equivalent of the original binary number. The register is initially set to a logical zero. The state of each stage is then rearranged during the loading of each word, dependent upon the presence or absence of a set input trigger which, in turn, is dependent upon whether the individual control gate is enabled or inhibited by the inverted comb filter outputs at I-15-34, I-15-33, and I-15-27. A pulse is then introduced at the register input I-2-22, followed 15 microseconds later by the clock pulses which are simultaneously counted by the decimal counter. A stop pulse is generated when the number of counts introduced to the register results in a positive output from the final stage of the BC group representing the word. For

example, if the three binary outputs from the comb filter are representative of the number zero, the complement, a logical one, will enable the set input "nand gates" during the period of a negative control pulse at the other input to the gate. Consequently, each BC set output will be changed to a logical one state. The added count (start pulse) will then initiate the rearrangement of all the set outputs to the logical zero state, which will immediately generate a stop pulse. The counter, therefore, will readout a decimal zero. Another example is presented by the register timing diagram of Figure 28 which describes the processing of a digital number representing C_5 and C_6. This number results in the "register proper" being loaded with the binary number 001001, having the decimal equivalent of 9. This diagram, however, shows 36 clock pulses being required to clear the register. This is a result of two stages of multiplication by two per stage preceding the register.

Three binary counter stages having outputs at III-18-20, III-18-27, and III-18-18 are shown, with their associated control gates, in Figure 8. These stages serve to multiply, where appropriate, each digital number by a prescribed factor which will result in the decimal counter reading out the equivalent number to that stored in the encoder binary counters, thereby avoiding the task of manual conversion. The number stored in the encoder binary counters is larger than its representation during low speed data for both C_{1-4} and C_{5-6} and during high speed data for C_{1-4}. This is due to the difference in the number of binary counter stages being employed to represent these numbers, and is explained in the report entitled "Proposed Requirements for Satellite S-51 Test Stand Telemeter Reduction System"

2. Clock and decimal counter start control

A start or "read" command pulse is generated at the appropriate time for each readout of the accumulated data. This pulse appears at the "nand gate" output I-14-21 and serves to initiate a decimal counter start pulse at III-9-7; to present the "additional count" to the register through I-12-31; and to trigger the delay multivibrator input at I-13-25. The output pulse at I-13-17 is delayed from the initiating start pulse by 15 microseconds to allow sufficient time for the added count to rearrange the register. The delayed pulse is then "gated" out at I-12-16 unless the "nand gate" is inhibited by the presence of a positive stop pulse at I-12-11 which will only occur when the digital number being "read out"

is equal to zero. Flip-flop output I-11-28 will be switched to its negative state by the presence of the delayed start pulse at I-11-25, which enables the "nand gate" at input I-14-16 during the period of each clock pulse present at I-14-14. The delay multivibrator input at I-13-22 receives a trigger for each clock pulse, resulting in an output to the register input logic from I-13-29 and to the decimal counter from I-13-10.

3. Clock and decimal counter stop control.

A negative pulse will appear at the "nor gate" output I-14-13 at the completion of each digital word readout. This pulse is then inverted at I-10-34 and serves as a trigger pulse to the delay multivibrator input I-9-9. The trailing or positive going edge of the output pulse at I-9-17 then triggers the delay multivibrator at input II-1-25. The outputs at II-1-6 and II-1-31 present a stop pulse to the decimal counter and a reset pulse to the register multiplier binary counter stages, respectively. A positive pulse is presented to the "flip-flop" set input I-11-20 which results in the reset output I-11-28 being returned to its logical zero or positive state. This, in turn, inhibits the clock gate at input I-14-16, thereby removing the input pulses to the register and decimal counter until the next read command pulse occurs.

The enabling inputs to the "nor gate" I-14-13 are controlled by three "nand gates" having outputs at I-10-33, I-10-27, and I-10-12. Each of these gates is controlled by two inputs such that only one gate is enabled during the readout of each digital number. One input of each gate is controlled by the reset output of a separate "flip-flop" and receives an enabling condition only during the read-out of one of the possible three digital numbers. The other input to each of the gates is received from a ten microsecond delay multivibrator output which is triggered from the set output of the most significant binary counter stage representing the particular digital number being processed through the register.

G. Simulator Figures 20, 22, and 29

The circuitry required for developing the proper simulated signals for use in testing the operation of this system has been included as an integral part of the system. The signals generated include a continuous series of ten millisecond pulses having ten millisecond intervals to represent the channel "blank-burst" periods. Every sixteenth channel is represented by a fifteen millisecond pulse preceded by a five millisecond blank, which distinguishes channel "0" of each frame as the synchronization channel. The frequency of each channel burst is variable by front panel controls which facilitates testing of the

comb filter. Other signals presented are a series of negative pulses representing the 15.4 KC blank periods during low speed operation; a negative pulse representing the 4.5 KC comb filter output during high speed operation; and a negative pulse representing the 5 KC comb filter output during high speed operation on F(O) C(O).

The output of the free-running multivibrator at II-2-35 is a ten millisecond square wave as shown in Figure 29, which is combined with the "nor gate" input at II-5-29. This input is a six millisecond pulse which is generated at the delay multivibrator output II-4-29, after a delay of fifteen milliseconds introduced at the delay multivibrator output II-4-31. The initiating trigger occurs once, from the scale of sixteen counter output II-3-6, for every sixteen square wave inputs at II-3-22. The resulting output at II-5-27, therefore, simulates a frame of data channels between each synchronization channel.

The output at "nand gate" II-5-12 is presented through switch 2(A-3) to simulate the 15.4 KC blank envelope and is inverted at II-5-6 to serve as a gating pulse for the sine wave oscillator output.

Operation of the system using the simulator requires that switch number one be in the "test slow" position.

The scale-of-sixteen counter, having the input at II-6-22, serves as a frame counter to supply the frame bracket control pulses. The output at II-6-20 enables the "nand gate" II-5-16 during every other channel "0", thereby simulating the 4.5 KC envelope for high speed data. Similarly, the 15 millisecond 5 KC envelope output at II-4-17 is triggered from II-6-6 and occurs once per sequence or every sixteenth frame.

A simulated signal for testing the flywheel operation, during a period when there are missing "bursts" of data, is generated by inhibiting the "nand gate" at II-5-10 for a period of several "bursts". This is accomplished by placing switch number 11 (located on the back control panel) in the H.S. Test position and switch number 2 in the High Speed position.

H. Comb Filter Refer to Figures 30, 31, and 32

The comb filter is a series of 8 bandpass filters, each of which is tuned to a different frequency range. The comb filter converts the eight frequencies to the binary representation of octal numbers. This binary representation is shaped and buffered and the output of the comb filter is then loaded into the 15-bit register for conversion to its decimal equivalent.

The input to the comb filter is a square wave from the output of the AGC circuit in the Decommutator. The signal is clipped to approximately 0.2 volts, peak to peak, and a.c. coupled through a 47 microfarad (uf) capacitor to a transistor, Q_1, which is biased into its conducting state so that it passes the signal without further clipping. Transistor, Q_1, is an emitter-follower whose output is used as the input to the 10 filter-shaper boards.

The filter-shaper boards include eight bandpass filters, each of which is tuned to a different frequency bandwidth that represents an octal number, and two special purpose bandpass filters.

The frequency passband for each filter is as follows:

Octal No.	Binary output	Center Frequency (cps)	Lower Frequency limit (cps)	Upper Frequency limit (cps)
0	000			
1	001	5,601	5,457	5,745
2	010	6,225	6,062	6,388
3	011	6,957	6,767	7,147
4	100	8,016	7,799	8,233
5	101	9,256	8,992	9,520
6	110	11,196	10,808	11,584
7	111	14,158	13,667	14,641
		4,500	4,300	4,700
		15,400	15,100	15,900
		5,200	4,950	5,300

The ten filters are basically the same circuit; the only difference in them is a variation in the value of the reactive components of the resonant circuit and the frequency band for which they are tuned. Therefore, the discussion that follows applies equally well to all ten of the filter-shaper boards.

Transistors Q_2 and Q_3 are emitter followers that have been cascaded so as to increase their effective input impedance and to decrease their effective output impedance. Transistor Q_3 provides positive feedback through a 56K resistor to the tuned L-C circuit to increase the selectivity (decrease the frequency bandwidth) of the tuned circuit.

The output of transistor Q_3 is a.c. coupled through a .0068 uf capacitor. The silicon diode 1N251 blocks the negative portion of the signal and also the first 0.5 volt of the positive portion in order to prevent any extraneous signals from triggering Q_4. Transistor Q_4 is biased to be normally conducting and the

positive signal from Q_3 causes it to stop conducting. The Bourns 10 K Trimpot provides adjustment for desired frequency bandwidth. However, because of differences in transistors, it may also be necessary to change the 33 K resistor to obtain the desired frequency bandwidth. The silicon diode 1N251 in the collector circuit of transistor Q_4 and the 0.33 uf capacitor form a half wave detector so that the drive for Q_5 is a detected burst envelope if the frequency of that burst fell in the passband of that filter. Transistor Q_5 is used as a saturating amplifier whose output is used to drive the diode matrix that converts the output to the binary representation of an octal number, or to drive an inverter amplifier directly. The matrix outputs are amplified by a transistor amplifier and these outputs are available at three BNC connectors (2^0, 2^1, and 2^2) on the front panel of the control panel. The amplified matrix outputs also form the inputs to the 15 bit register.

The comb filter output conditions for 2^0, 2^1, and 2^2 can be simulated when the switch on the front of the control panel is in the "Test" position. This is accomplished by supplying either 0 volts (2^0, 2^1, and 2^2) or -9 volts ($\overline{2}^0$, $\overline{2}^1$, and $\overline{2}^2$) at the outputs of the comb filter. The binary representation of the desired octal number is obtained through the three toggle switches on the front panel. An Octal-Decimal Conversion Table Figure 30 shows the decimal equivalent of any octal number (in binary form) that can be simulated by the comb filter.

VIII OPERATING PROCEDURES

A. Signal Input.

Two BNC connectors are provided on the rear control panel which are engraved "Tape and Receiver", respectively, under the main heading of "Signal In". The desired input is selected by a toggle switch mounted on the front control panel, which is correspondingly engraved. An access hole is provided in the rear of the cabinet for cabling to the connectors. The recommended input level is between 2 and 5 volts peak to peak.

B. Hewlett-Packard Connectors

1. Digital Channel:

Power switch -- on
Function selector -- Time interval
Time unit -- Ext.
Trigger slope -- Sep.
Start input -- minus
Stop input -- minus
Start trigger level -- AC(X1)
Start potentiometer -- full CCW (minus 3 volts)
Stop trigger level -- AC (X1)
Stop potentiometer -- full CCW (minus 3 volts)

Display time -- Min.
Frequency unit -- any setting
Manual gate -- any setting
Sensitivity -- any setting

2. Analog Channel:

Power switch -- on
Function selector -- 10 period average
Time unit -- microsecond
Display time -- Min.
All other controls -- any setting

C. Hewlett-Packard Printers

Power switches -- On
Record -- On when operator desires a print-out of data.
All other controls any setting

D. Comb Filter

Power switch -- On

E. Power Supply

Circuit breaker switch -- On
AC line switch -- On

F. Rack Power Switch -- On

G. Control Panel settings.

Power switch -- On
Signal In -- Operator's selection
Test Fast-Test Slow-operate switch -- Operate
Comb Filter control switch -- Operate
Channel Selector -- Operator's selection
Selects the channel to be processed through the analog channel system.

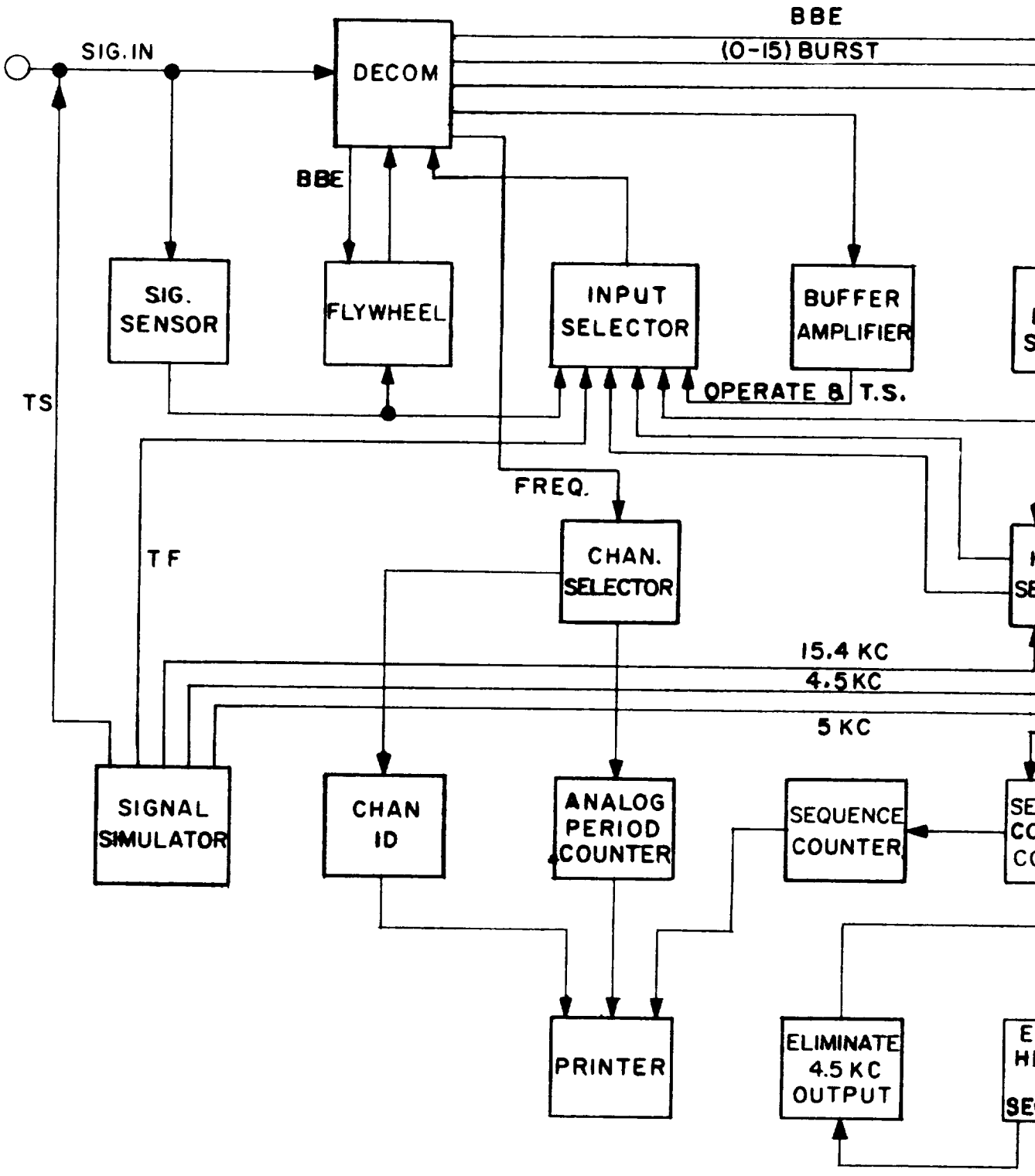
H. Decommutator

Power switch -- On
Burst-Blank Freq. -- Freq.
3 toggle switches engraved "High-Low"--All in the low position
Clippers -- adjusted so that the signal, viewing at clipper test point, is clipped evenly on both sides and so that the majority of the bursts have the same peak amplitude.

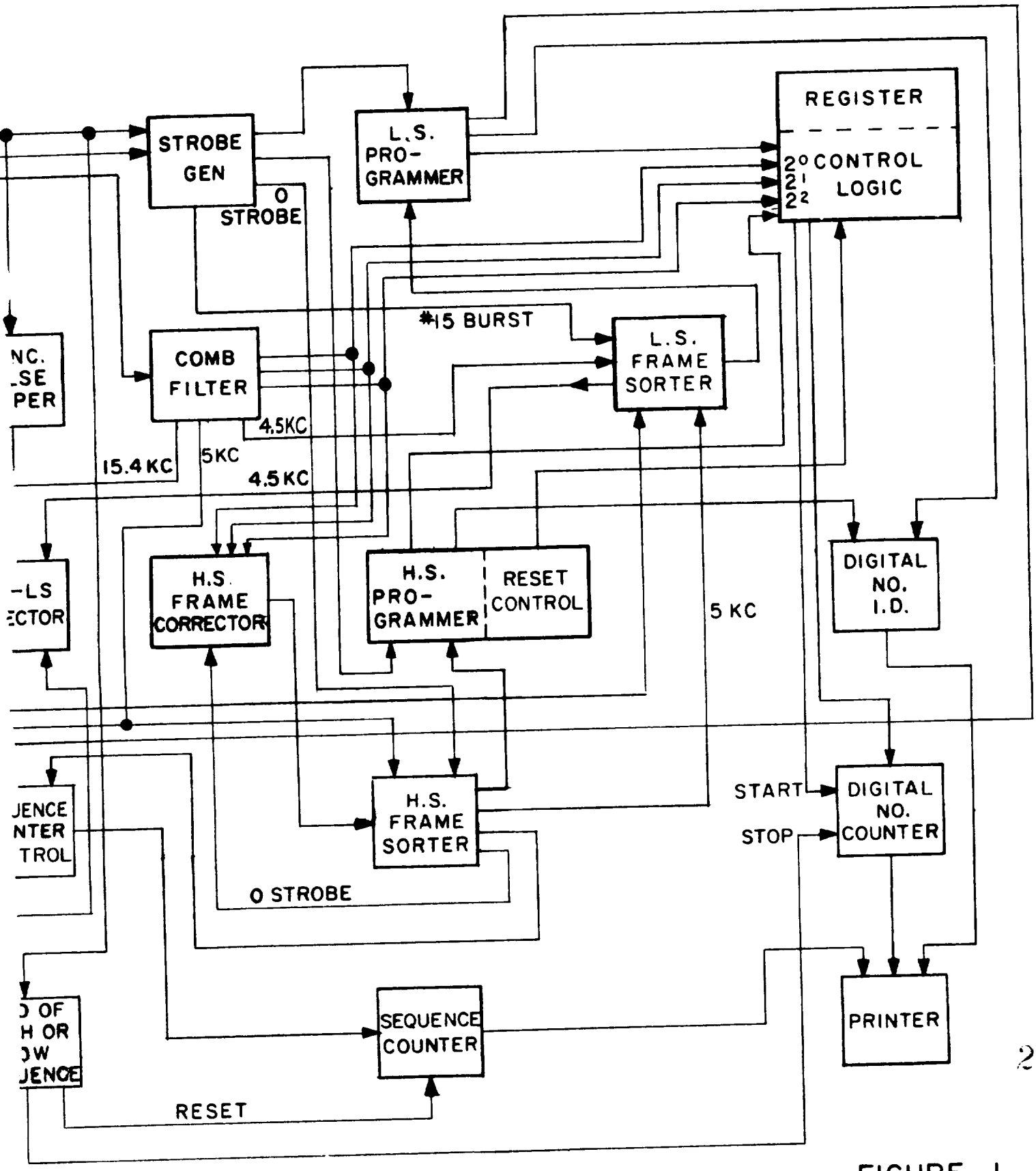
Output switch -- Selects channel burst appearing at the output BNC connector directly below switch. Operator will find this a convenient method for controlling synchronization of a test oscilloscope from this point.

Burst adjust, Blank adjust, and Sync adjust -- The three potentiometers should be initially set CCW. The burst Monostable multivibrator should be finally set for an output pulse duration of 9 milliseconds. The blank monostable multivibrator should be finally set for an output pulse duration of 4.5 milliseconds. The Sync. or FF-3 monostable multivibrator should be finally set for an output pulse duration of 14 milliseconds. These adjustments are fully described in appendix I.

S-51 TEST STAND



DATA REDUCTION SYSTEM



28

FIGURE 1

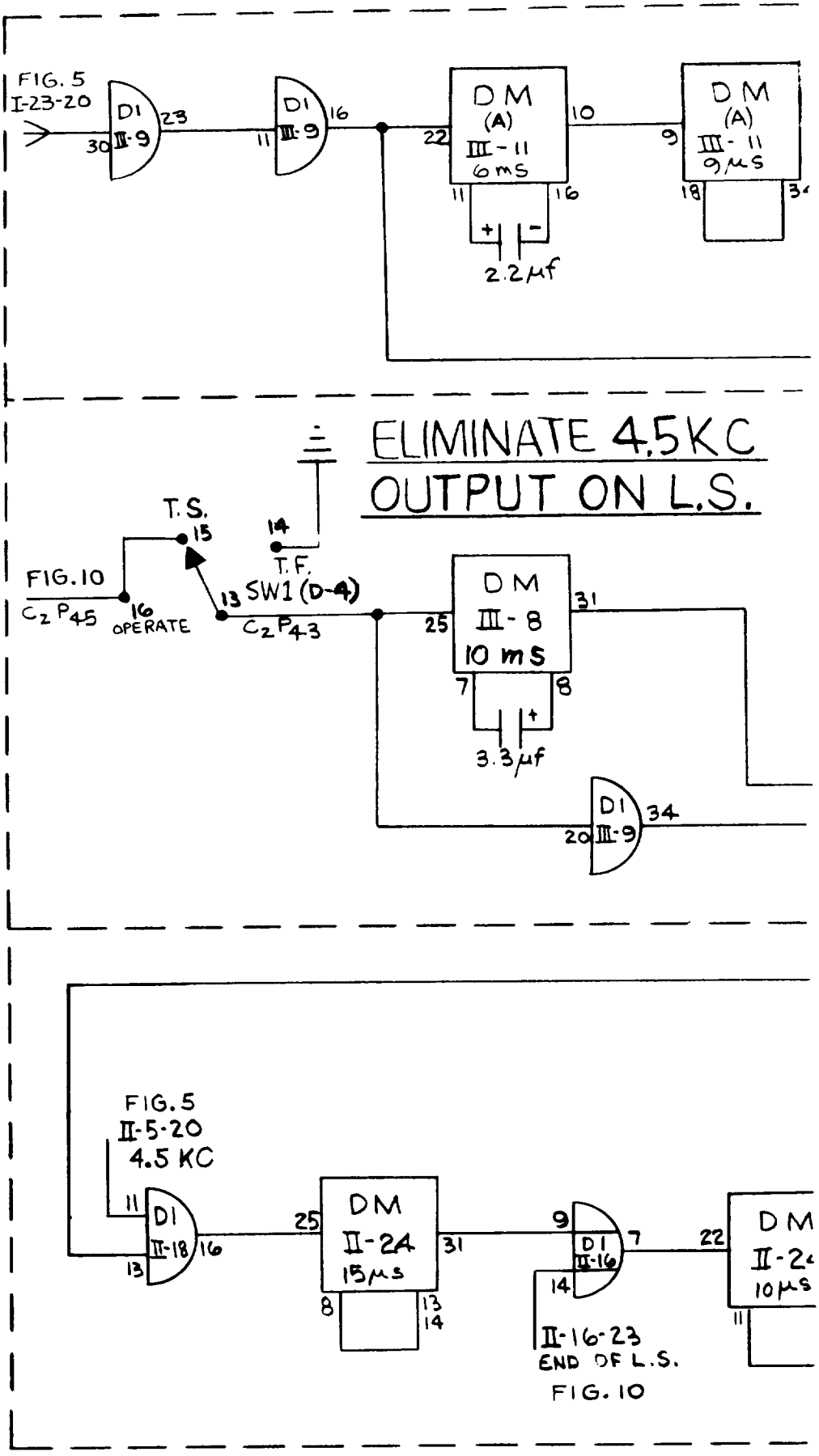
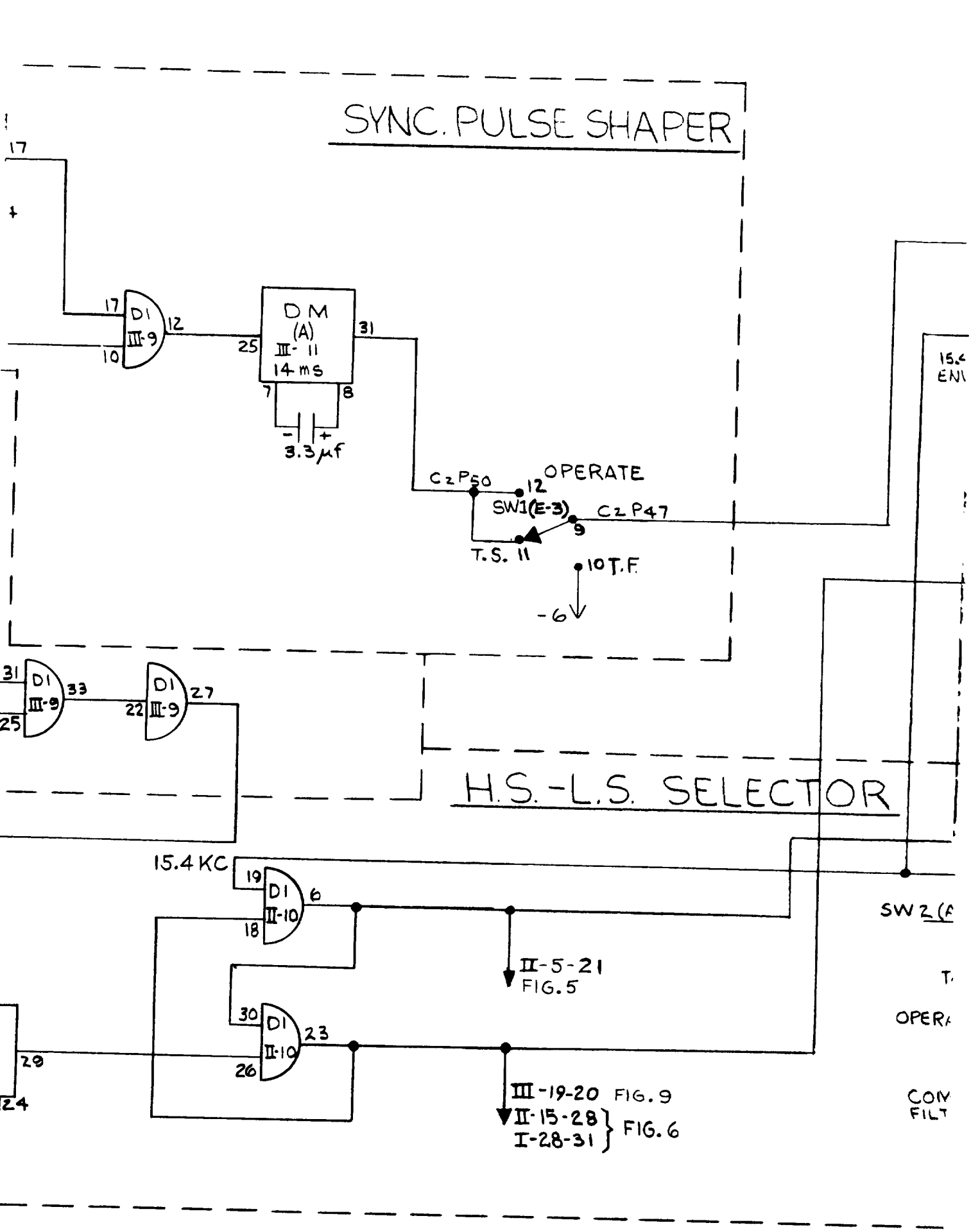
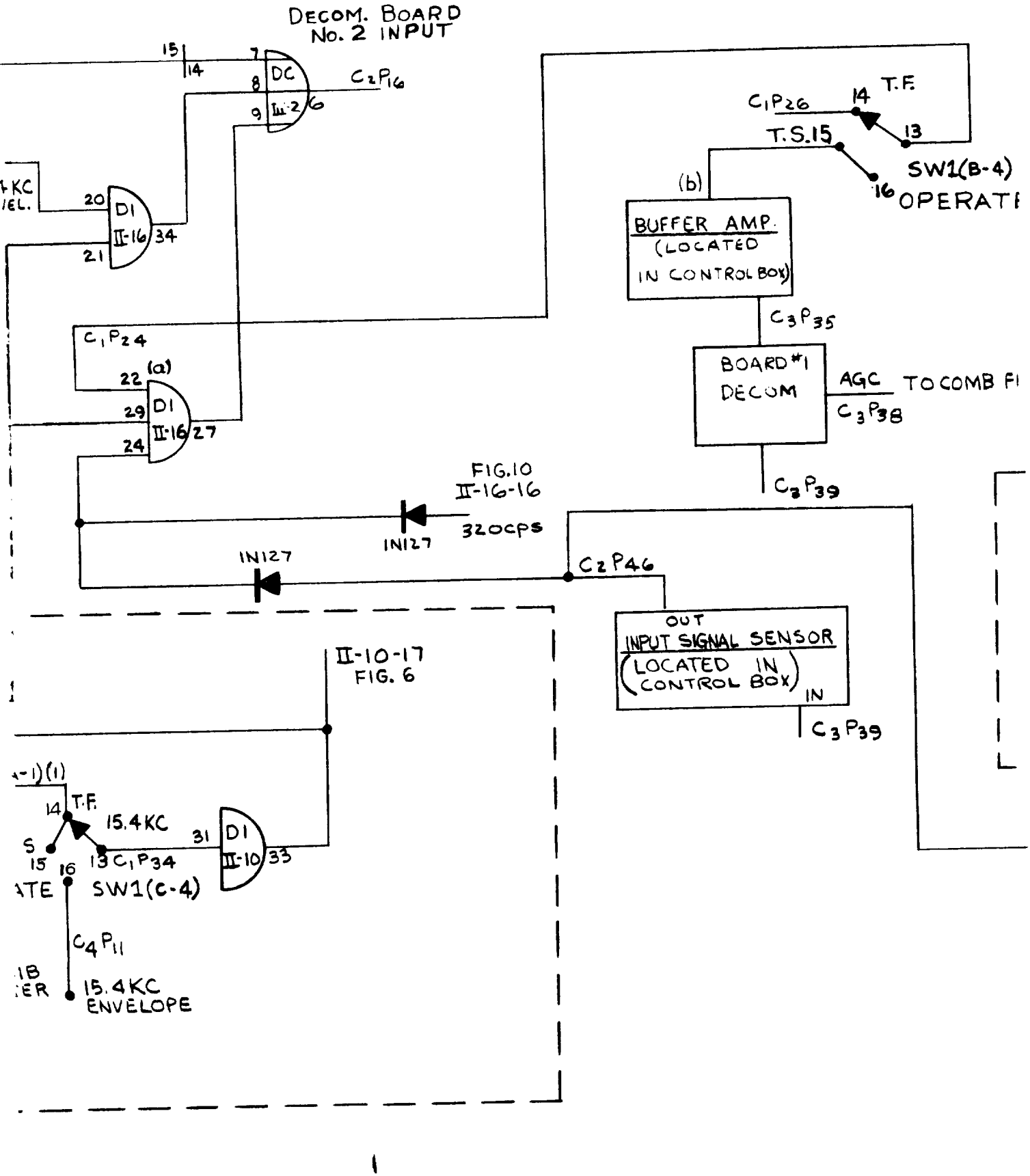
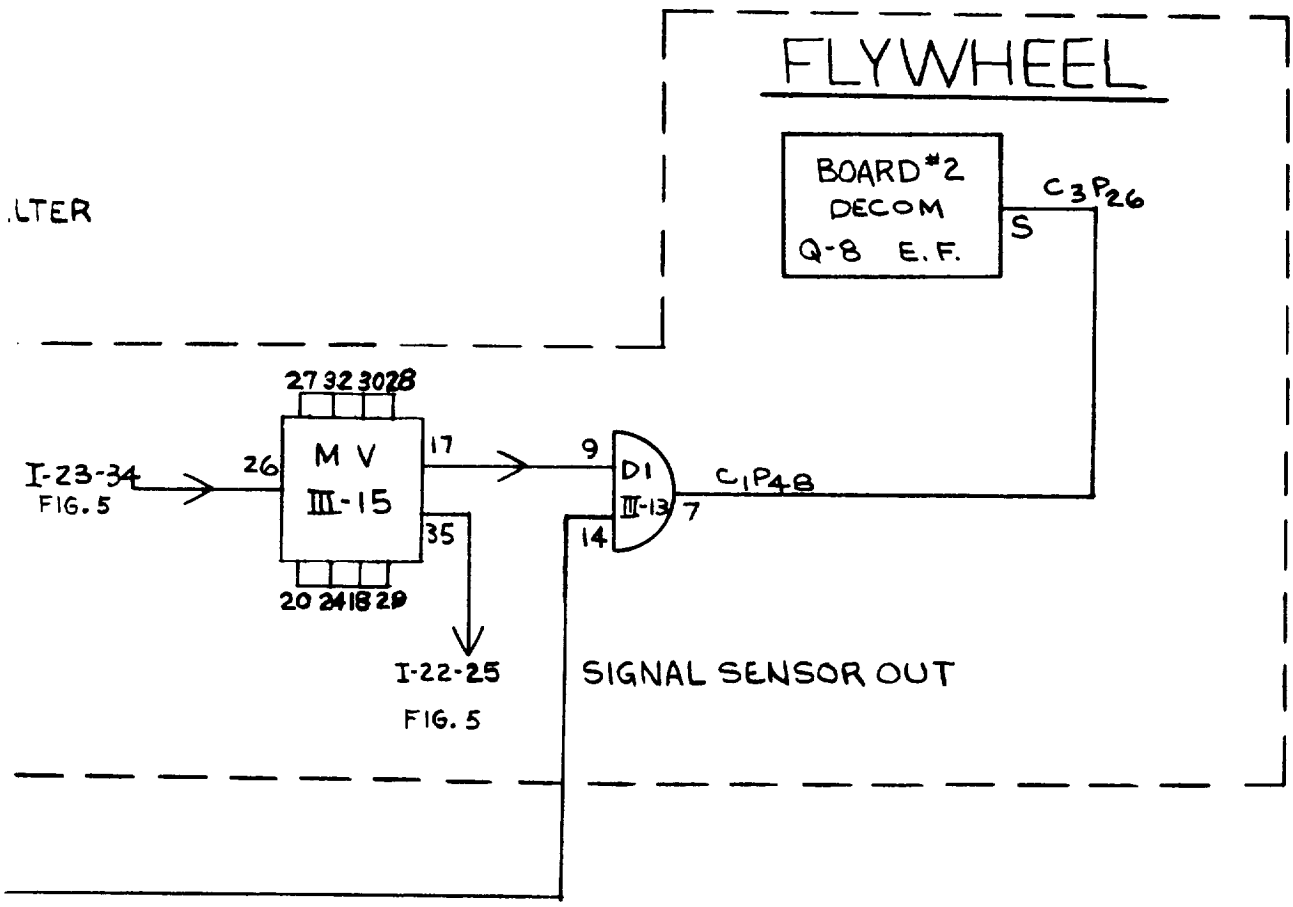


FIG. 5
I-23-20
D1
III-9
23
30
D1
III-9
16
11
DM
(A)
III-11
6 ms
22
10
11
16
+
-
2.2 μf
DM
(A)
III-11
9 μs
9
18
ELIMINATE 4.5KC
OUTPUT ON L.S.
T.S.
15
14
T.F.
FIG. 10
C2 P45
16
OPERATE
13
SW1 (D-4)
C2 P43
DM
III-8
10 ms
25
31
7
8
+
3.3 μf
D1
III-9
20
34
FIG. 5
II-5-20
4.5 KC
11
D1
II-18
16
13
DM
II-24
15 μs
25
31
8
13
14
D1
II-16
9
7
14
II-16-23
END OF L.S.
DM
II-2
10 μs
22
11
FIG. 10


SYNC. PULSE SHAPER
17
17
D1
III-9
12
10
DM
(A)
III- 11
14 ms
25
31
7
8
3.3 μf
C2P50
12
OPERATE
SW1(E-3)
C2P47
9
T.S. 11
10 T.F.
-6
31
D1
III-9
33
25
D1
III-9
27
22
H.S.-L.S. SELECTOR
15.4 KC
19
D1
II-10
6
18
II-5-21
FIG. 5
30
D1
II-10
23
26
29
24
III-19-20 FIG. 9
II-15-28
I-28-31
FIG. 6
SW 2 (A
T.
OPERA
CON
FILT

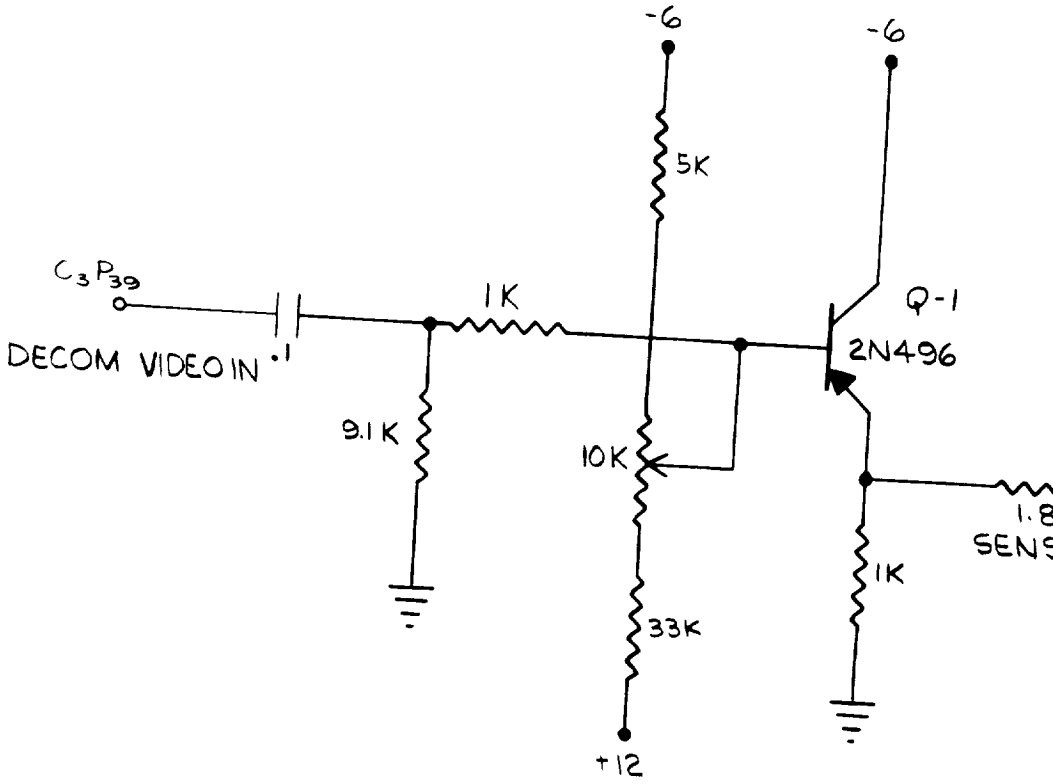
INPUT SELECTOR




FLYWHEEL
BOARD #2
DECOM
Q-8 E.F.
C3P26
S
27 32 30 28
MV
III-15
26
17
35
20 24 18 29
I-23-34
FIG. 5
9
D1
III-13
7
14
C1P48
I-22-25
FIG. 5
SIGNAL SENSOR OUT

S - 51 FIGURE 2

IN


-6
-6
5K
C3P39
DECOM VIDEO IN
.1
1K
Q-1
2N496
9.1K
10K
1.8
SENS
1K
33K
+12

MINIMU

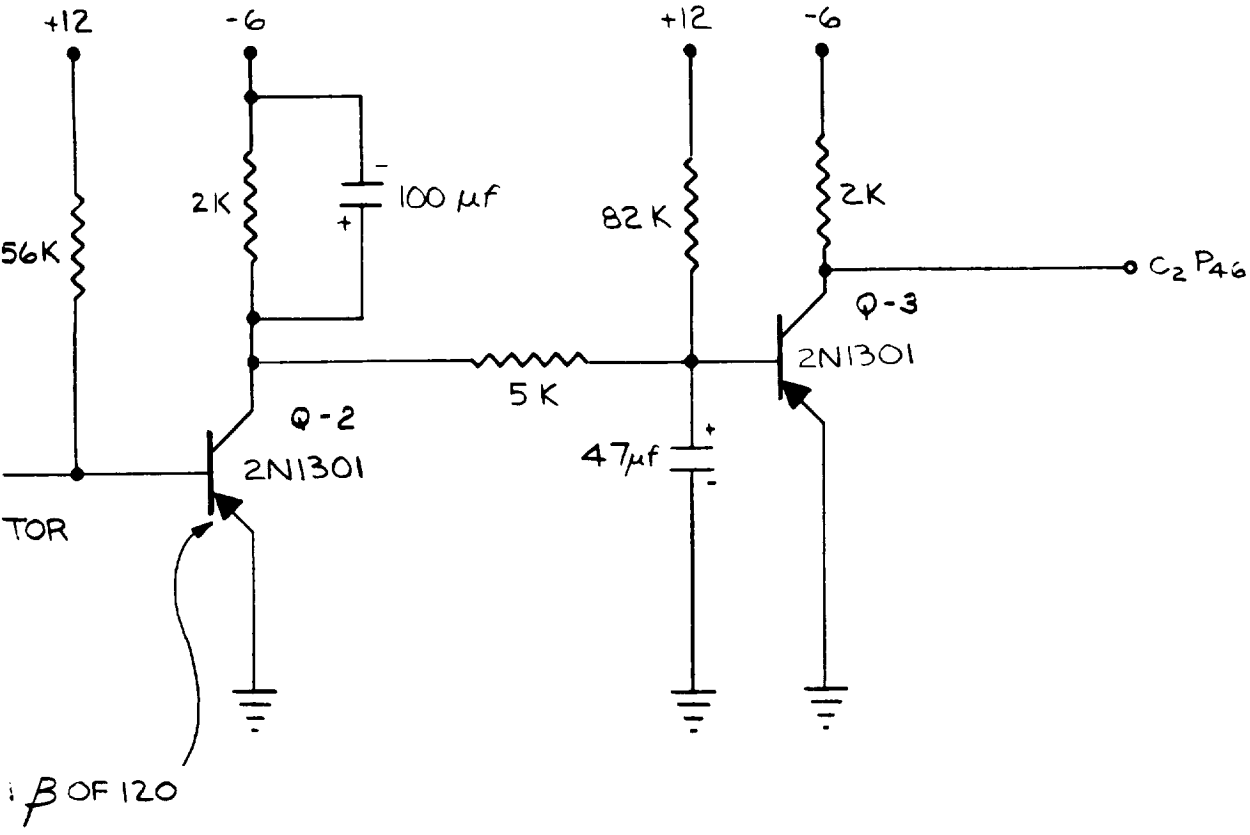
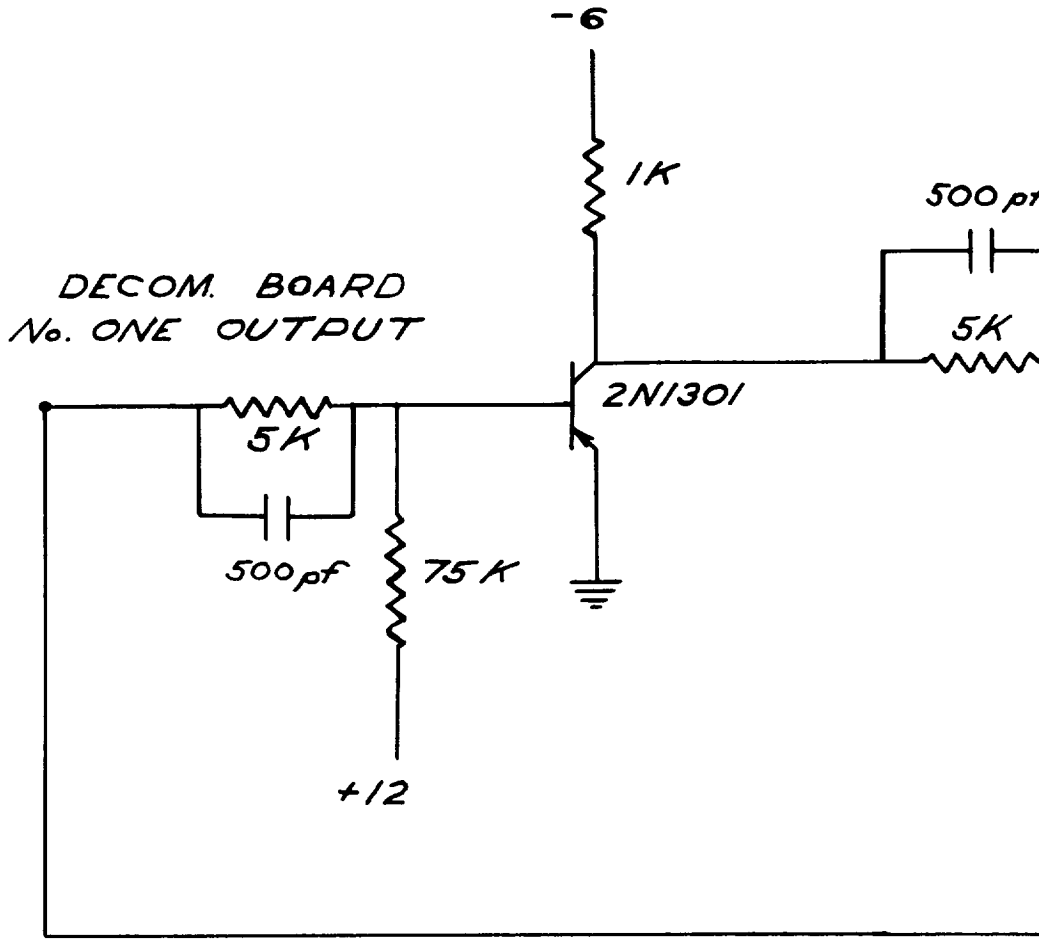
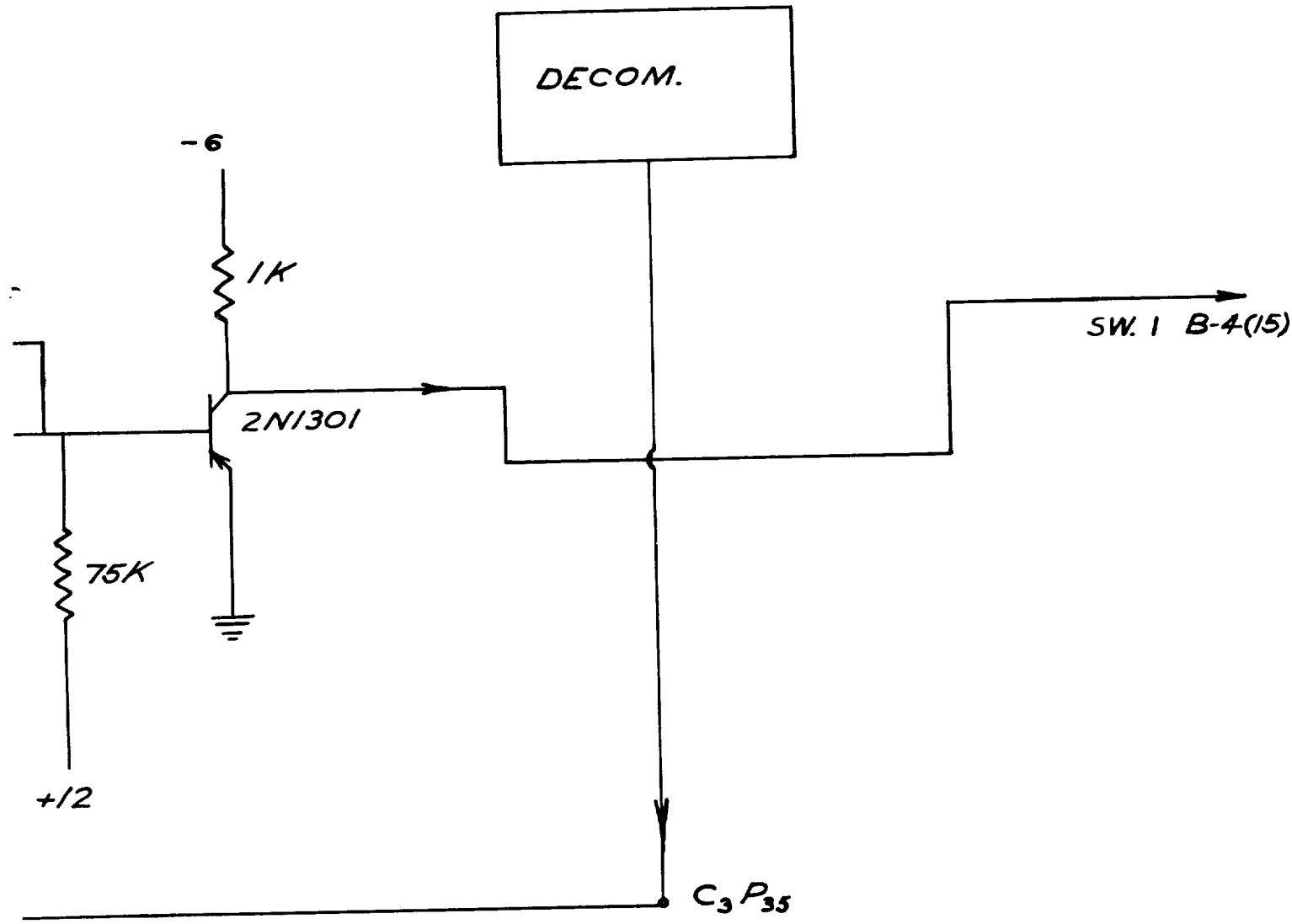

+12
-6
+12
-6
2K
100 μf
82K
2K
56K
C_2 P_{46}
Q-3
2N1301
5K
Q-2
2N1301
47μf
TOR
β OF 120

FIGURE 3

BUF



FER AMPLIFIER



S-51

FIGURE 4

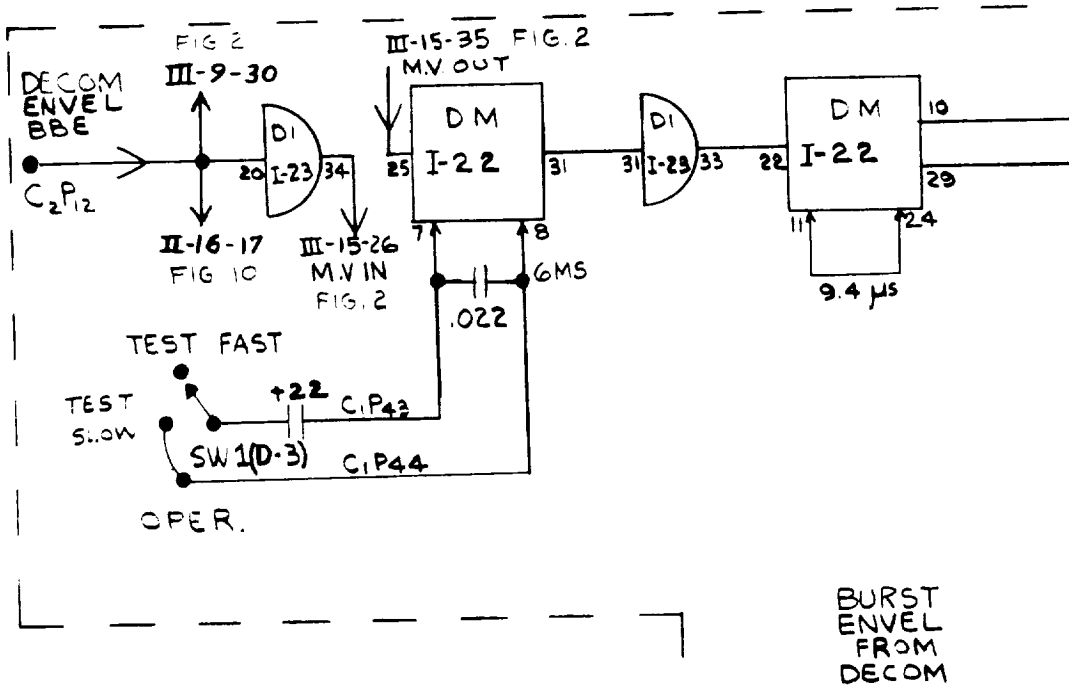
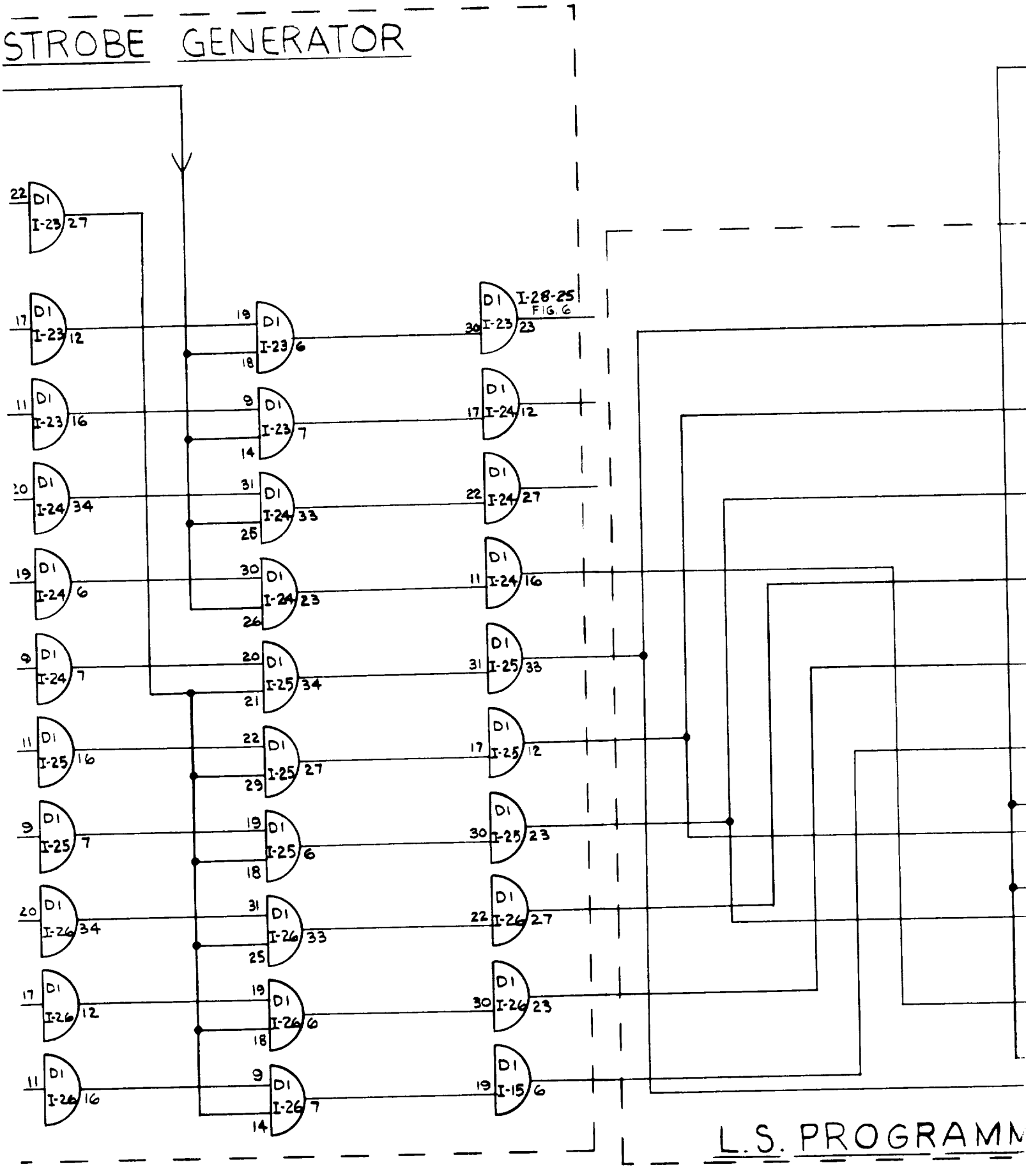
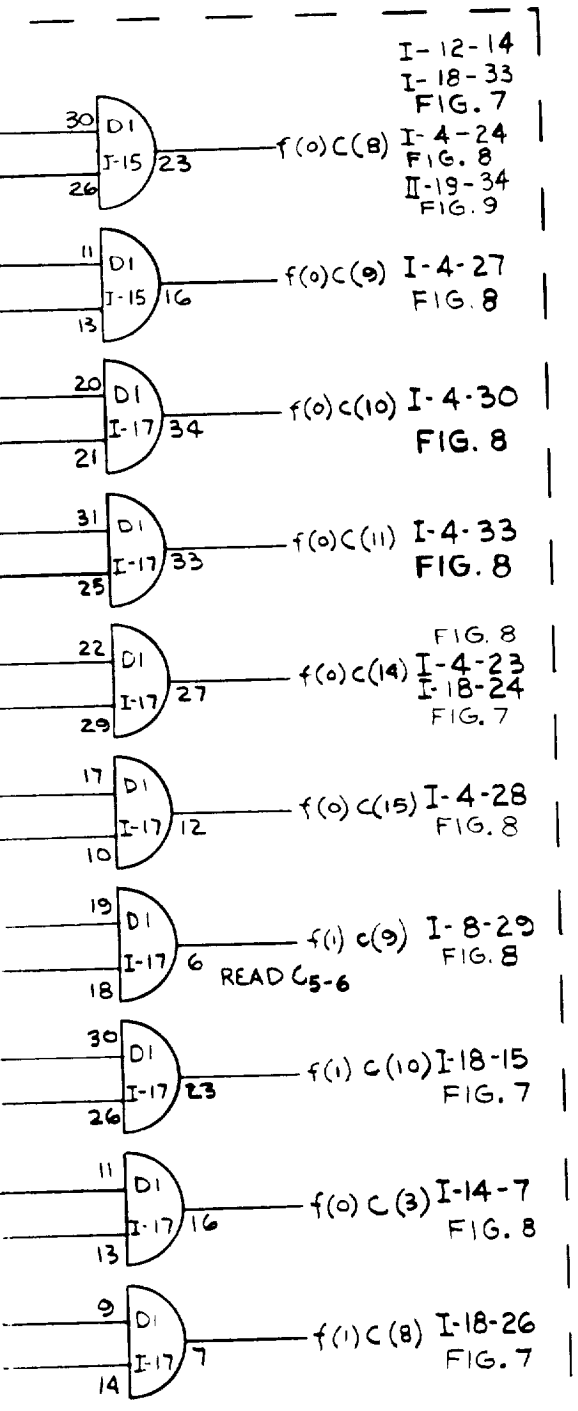
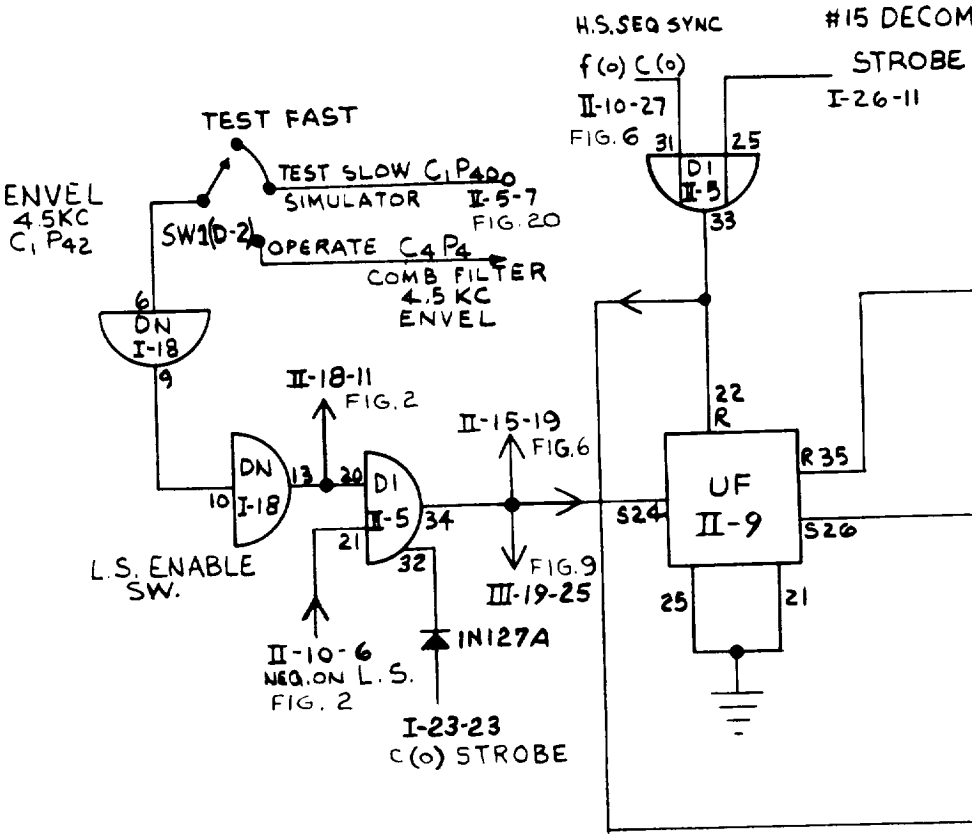


FIG 2
III-9-30
DECOM
ENVEL
BBE
C2P12
DI
I-23
20
34
II-16-17
FIG 10
III-15-26
M.V IN
FIG. 2
III-15-35 FIG. 2
M.V OUT
DM
I-22
25
31
7
8
.022
6MS
TEST FAST
TEST
SLOW
+22
C1P43
SW 1(D-3)
C1P44
OPER.
DI
I-23
31
33
22
DM
I-22
10
29
11
24
9.4 μs
BURST
ENVEL
FROM
DECOM

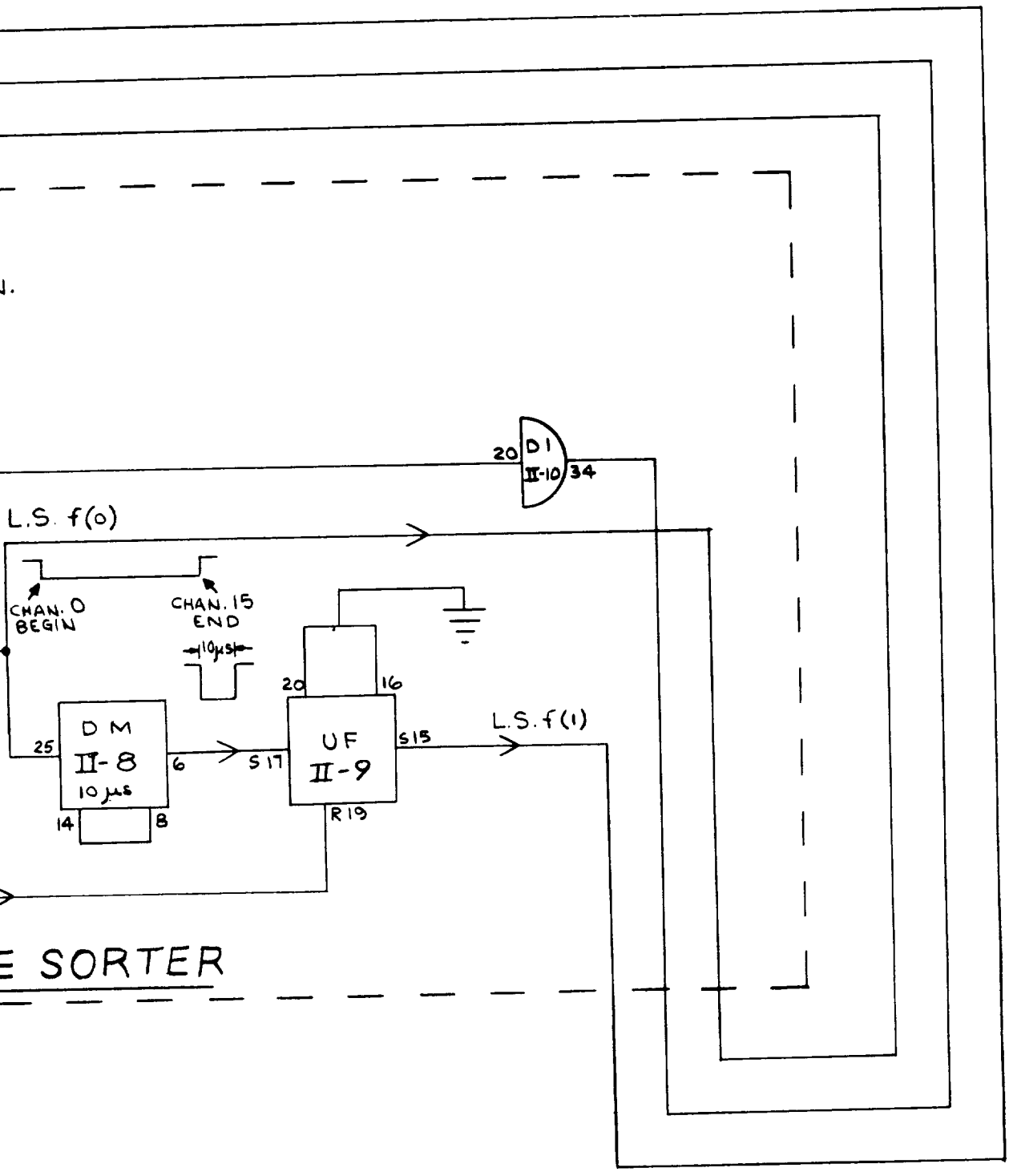
STROBE GENERATOR



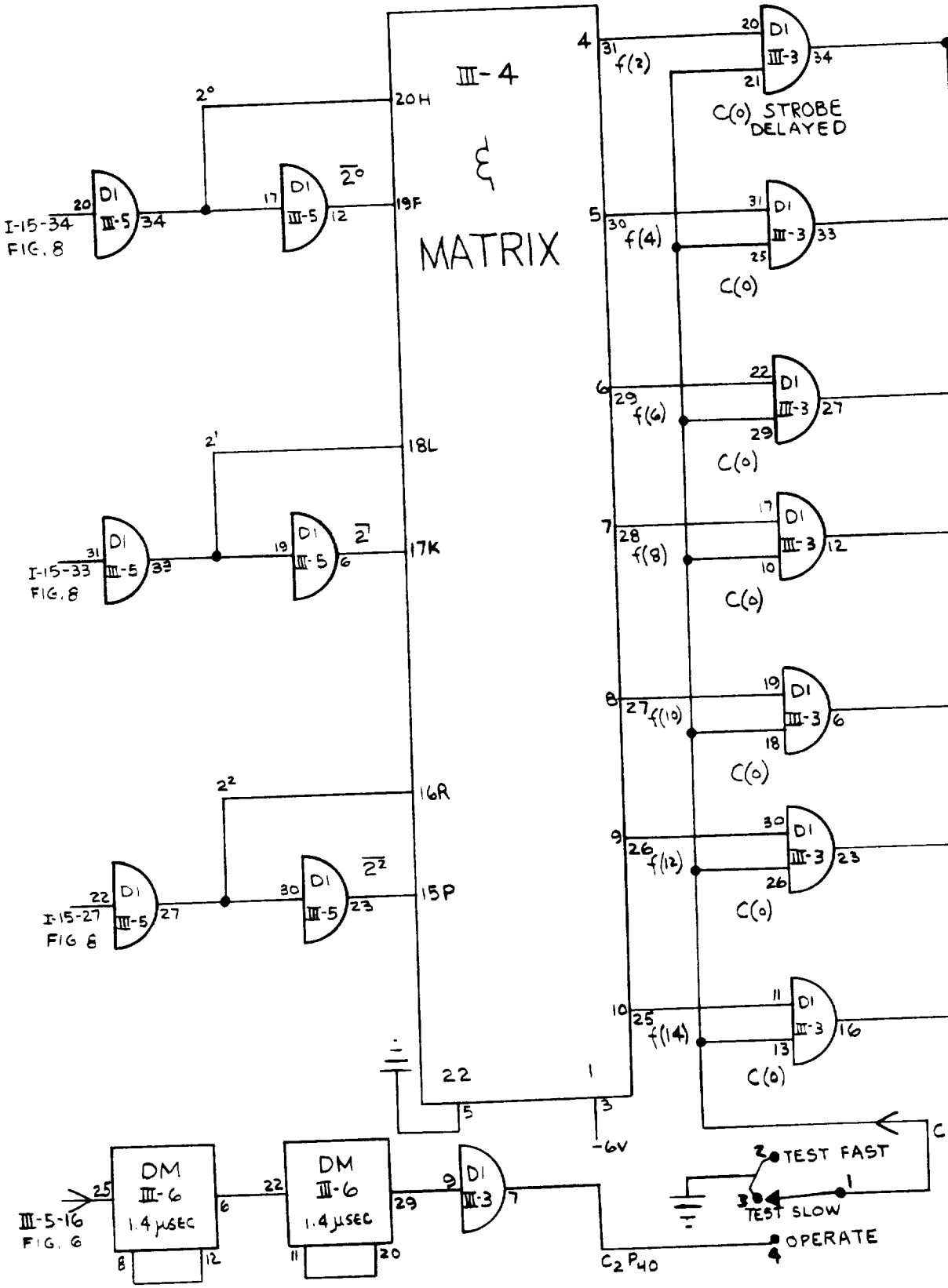

I-12-14
I-18-33
FIG. 7
30 D1 I-15 23 f(0) C(8) I-4-24 FIG. 8 II-19-34 FIG. 9
26
11 D1 I-15 16 f(0) C(9) I-4-27 FIG. 8
13
20 D1 I-17 34 f(0) C(10) I-4-30 FIG. 8
21
31 D1 I-17 33 f(0) C(11) I-4-33 FIG. 8
25
FIG. 8
22 D1 I-17 27 f(0) C(14) I-4-23 I-18-24 FIG. 7
29
17 D1 I-17 12 f(0) C(15) I-4-28 FIG. 8
10
19 D1 I-17 6 f(1) C(9) I-8-29 FIG. 8
18
READ C5-6
30 D1 I-17 23 f(1) C(10) I-18-15 FIG. 7
26
11 D1 I-17 16 f(0) C(3) I-14-7 FIG. 8
13
9 D1 I-17 7 f(1) C(8) I-18-26 FIG. 7
14


H.S. SEQ SYNC
f(0) C(0)
II-10-27
FIG. 6
#15 DECOM
STROBE
I-26-11
TEST FAST
TEST SLOW C1P4D0
SIMULATOR II-5-7
FIG. 20
ENVEL
4.5KC
C1 P42
SW1(D-2)
OPERATE C4 P4
COMB FILTER
4.5 KC
ENVEL
31 D1 II-5 25
33
6 DN I-18
9
II-18-11
FIG. 2
II-15-19
FIG. 6
22
R
DN I-18 10
13 20 D1 II-5 34
21 32
UF
II-9
S24
S26
R35
25 21
L.S. ENABLE
SW.
FIG. 9
III-19-25
II-10-6
NEG. ON L.S.
FIG. 2
IN127A
I-23-23
C(0) STROBE

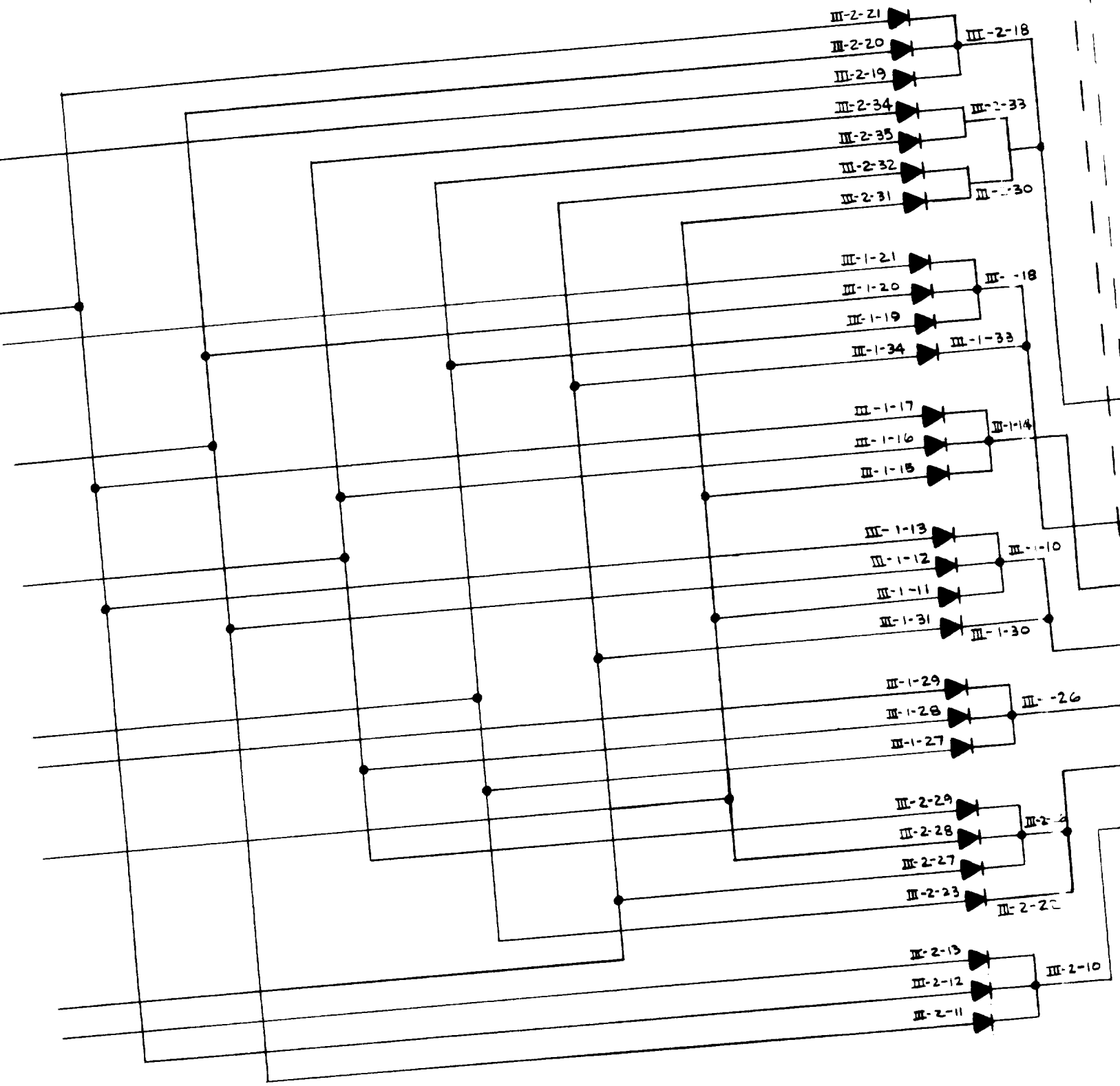
L. S. FRA


20
D1
II-10
34
L.S. f(0)
CHAN. 0
BEGIN
CHAN. 15
END
10μs
20
16
25
D M
II-8
10 μs
6
S17
UF
II-9
S15
L.S. f(1)
14
8
R19
E SORTER

S-51 FIGURE 5

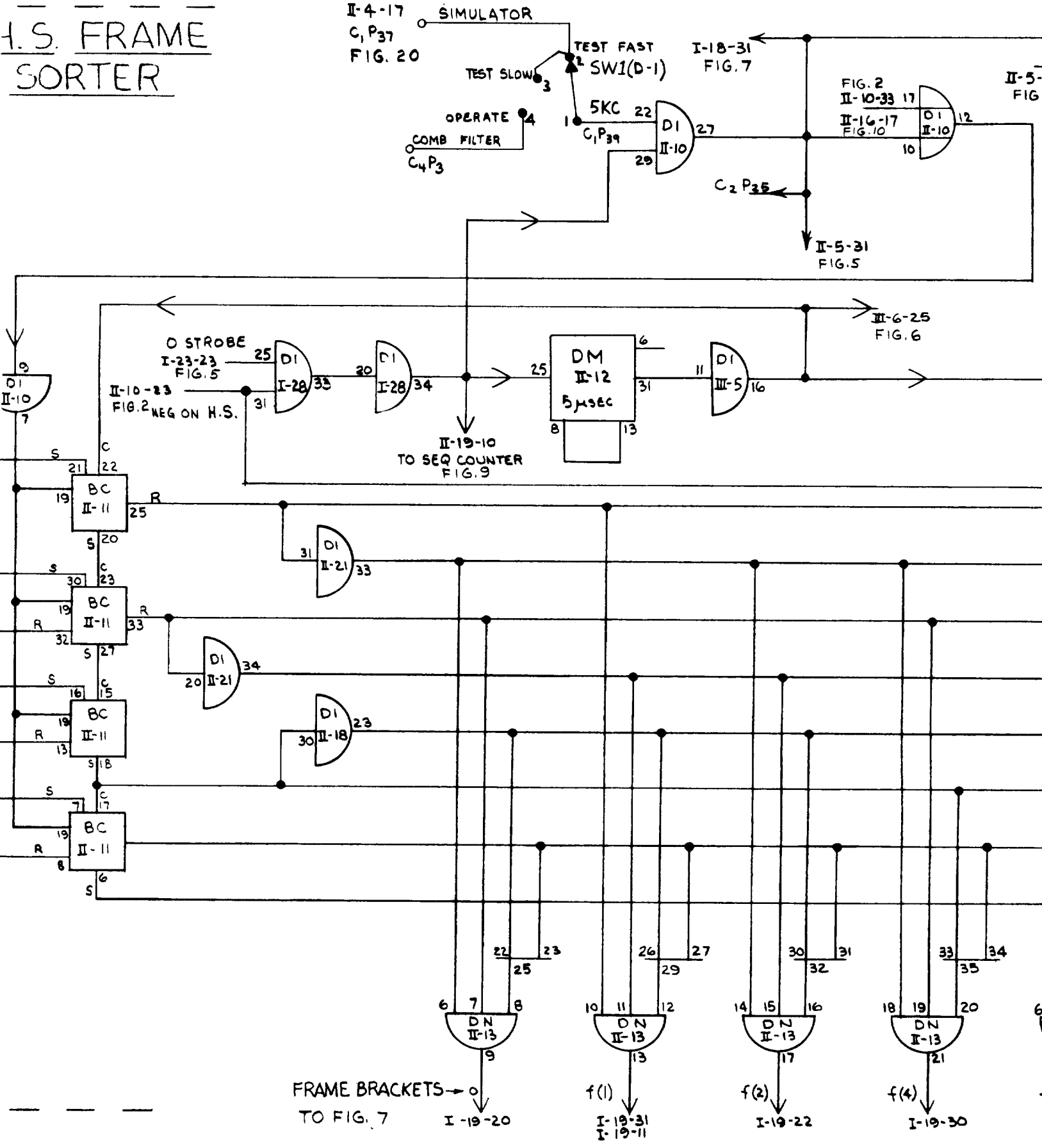

III-4
MATRIX
20H
19F
18L
17K
16R
15P
22
1
4
5
6
7
8
9
10
3
-6V
2°
2'
2²
$\overline{2^0}$
$\overline{2^1}$
$\overline{2^2}$
I-15-34
FIG. 8
I-15-33
FIG. 8
I-15-27
FIG 8
III-5-16
FIG. 6
DM III-6 1.4 μSEC
DM III-6 1.4 μSEC
D1 III-3
D1 III-5
f(2)
f(4)
f(6)
f(8)
f(10)
f(12)
f(14)
C(0) STROBE DELAYED
C(0)
TEST FAST
TEST SLOW
OPERATE
$C_2 P_{40}$

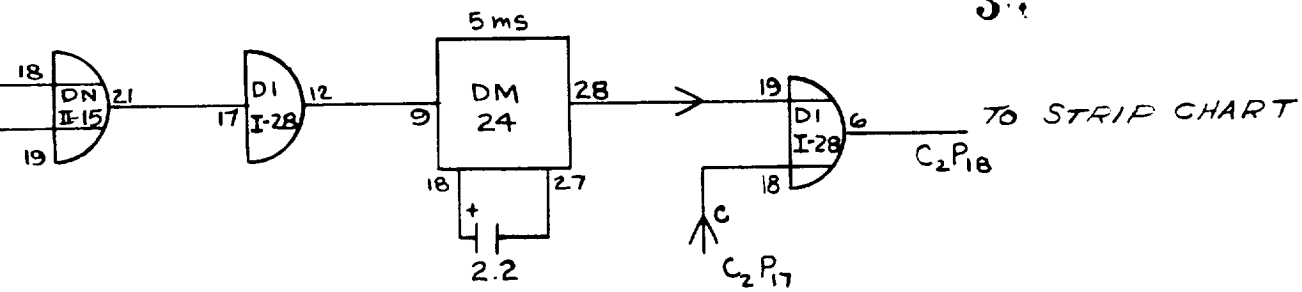
H.S. FRAME CORRECTOR

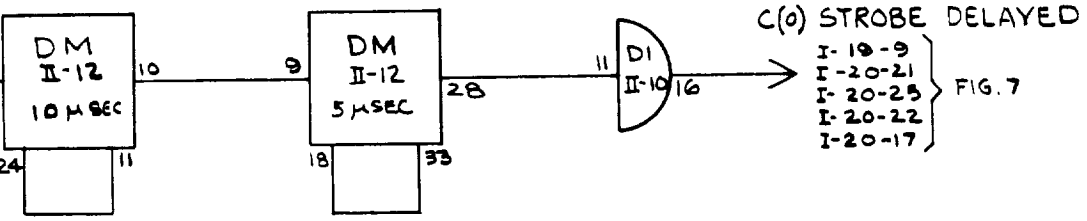


E-1)

H.S. FRAME SORTER




5 ms
DM 24
DI I-28
DN II-15
2.2
C
C_2P_{17}
C_2P_{18}
TO STRIP CHART


DM II-12 10 μSEC
DM II-12 5 μSEC
DI II-10
C(0) STROBE DELAYED
I-19-9
I-20-21
I-20-25
I-20-22
I-20-17
FIG. 7

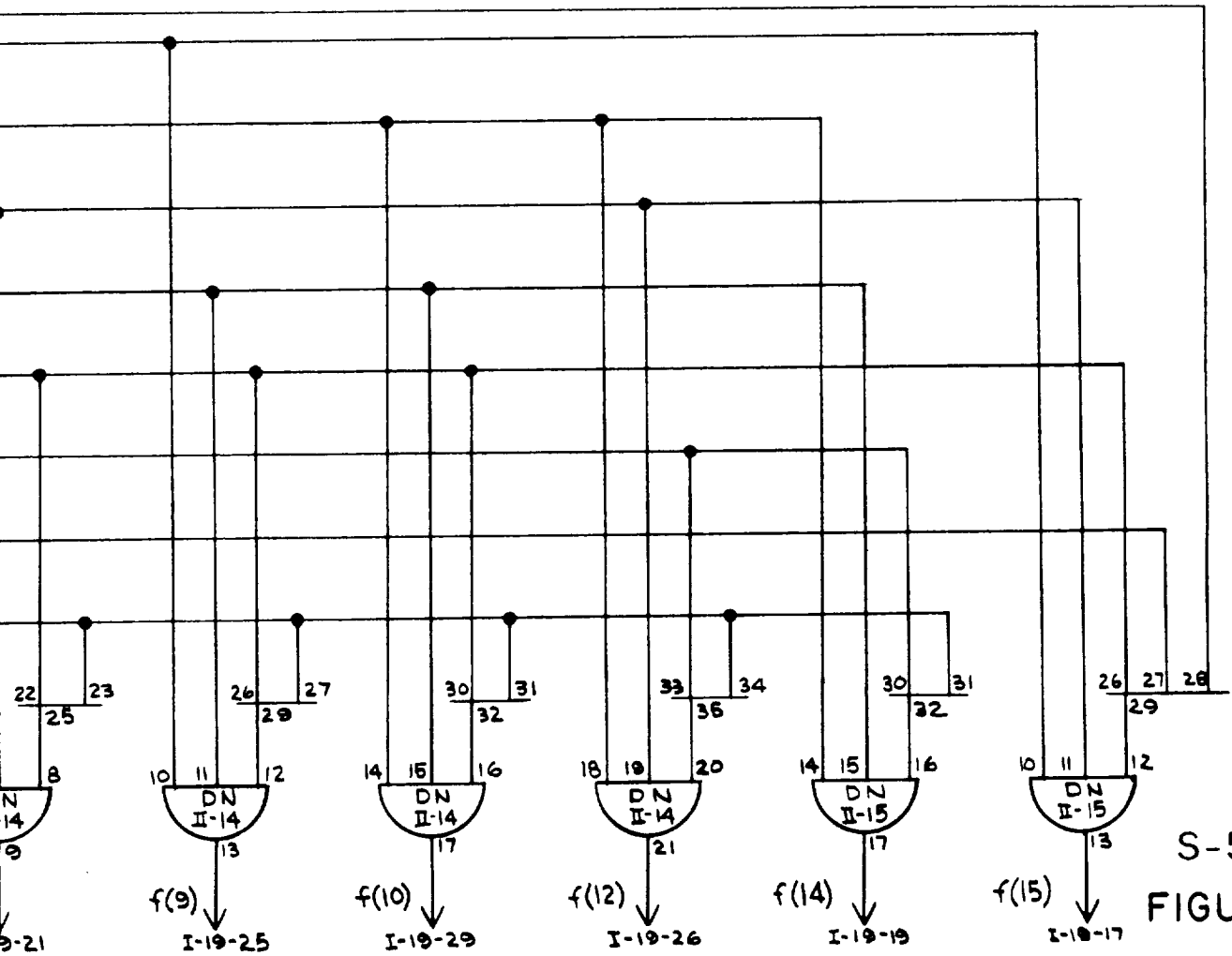

DN II-14
DN II-15
f(9)
f(10)
f(12)
f(14)
f(15)
I-19-25
I-19-29
I-19-26
I-19-19
I-19-17

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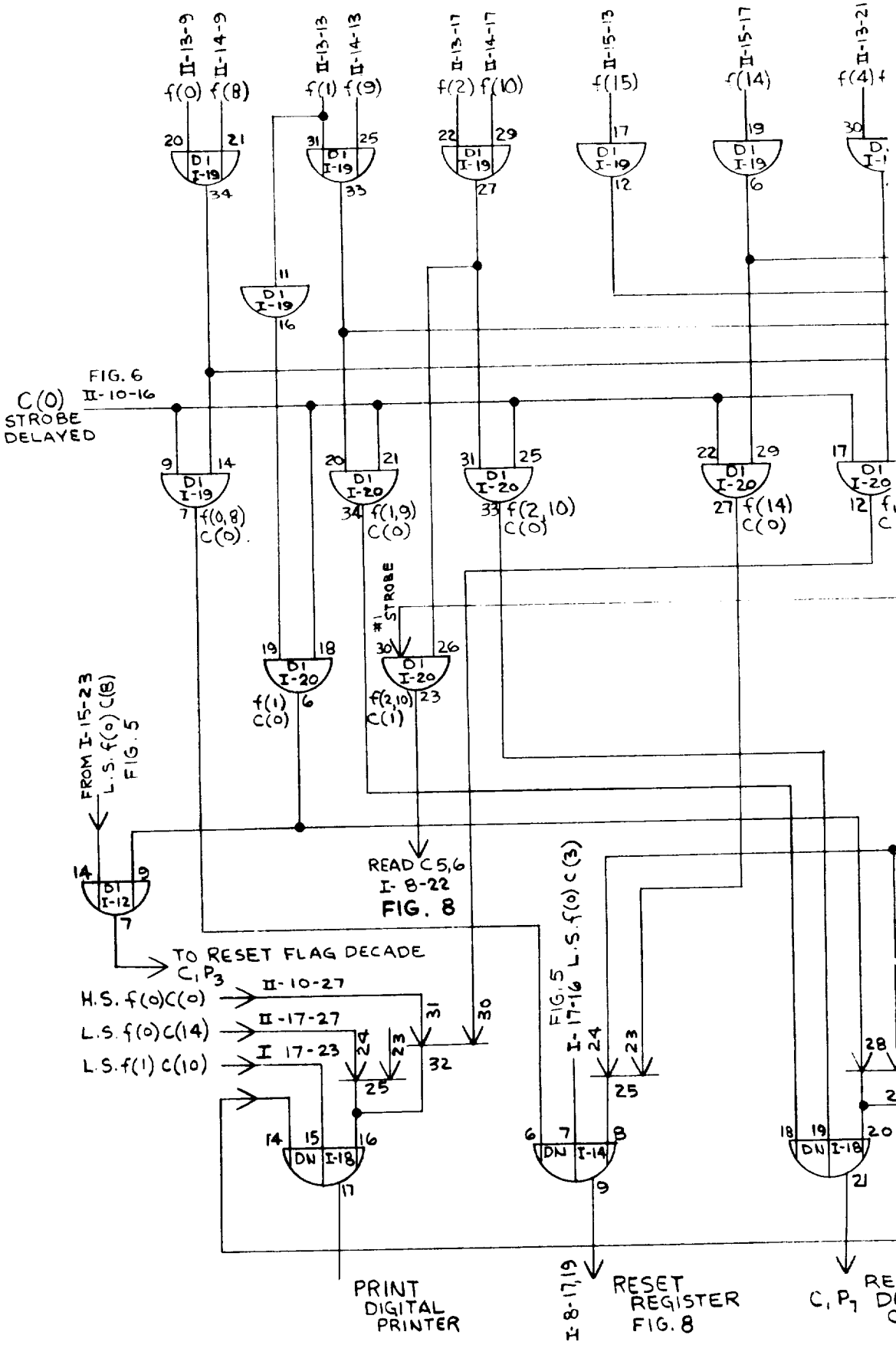
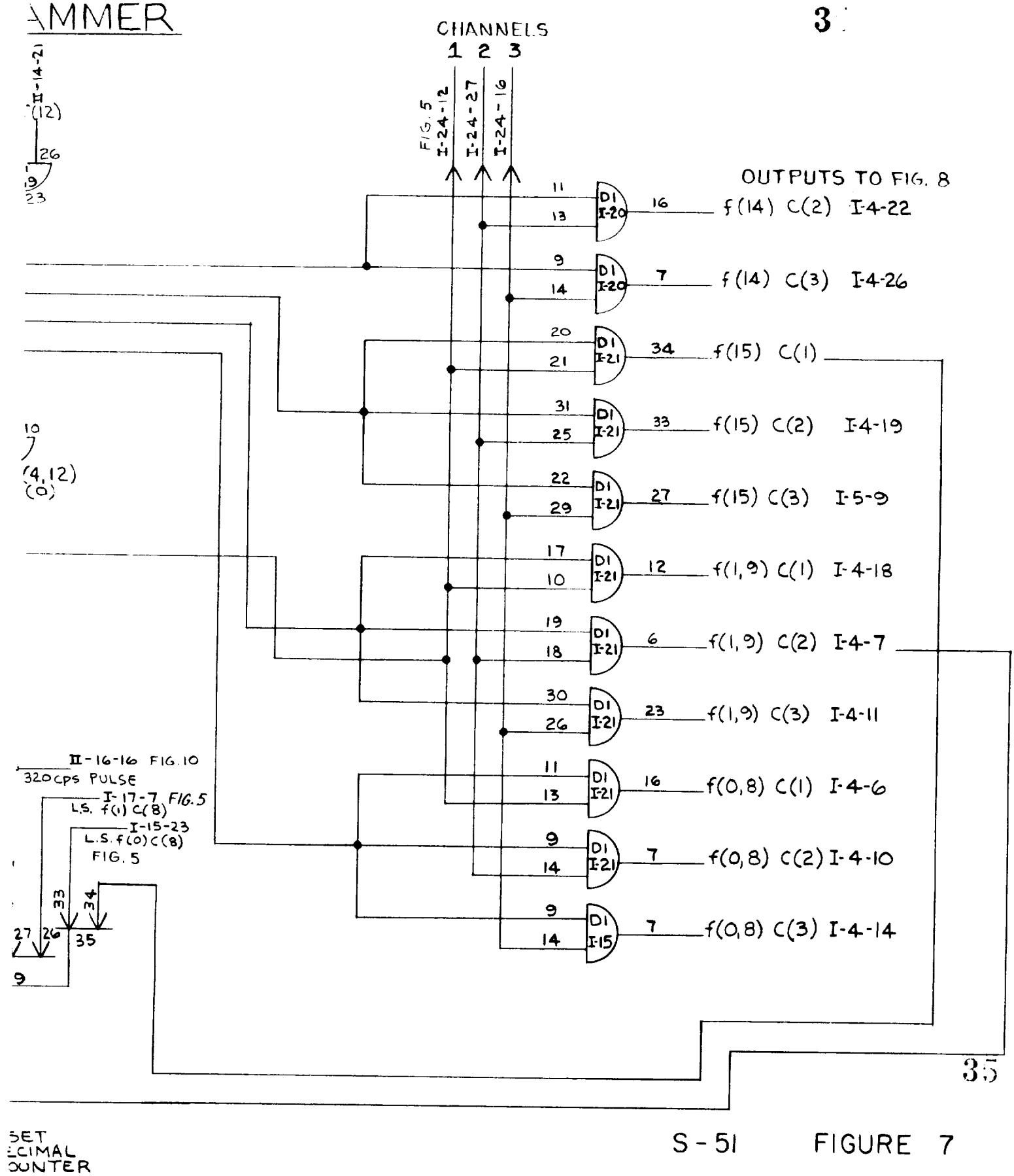
FIGURE 6

H.S. PROGR

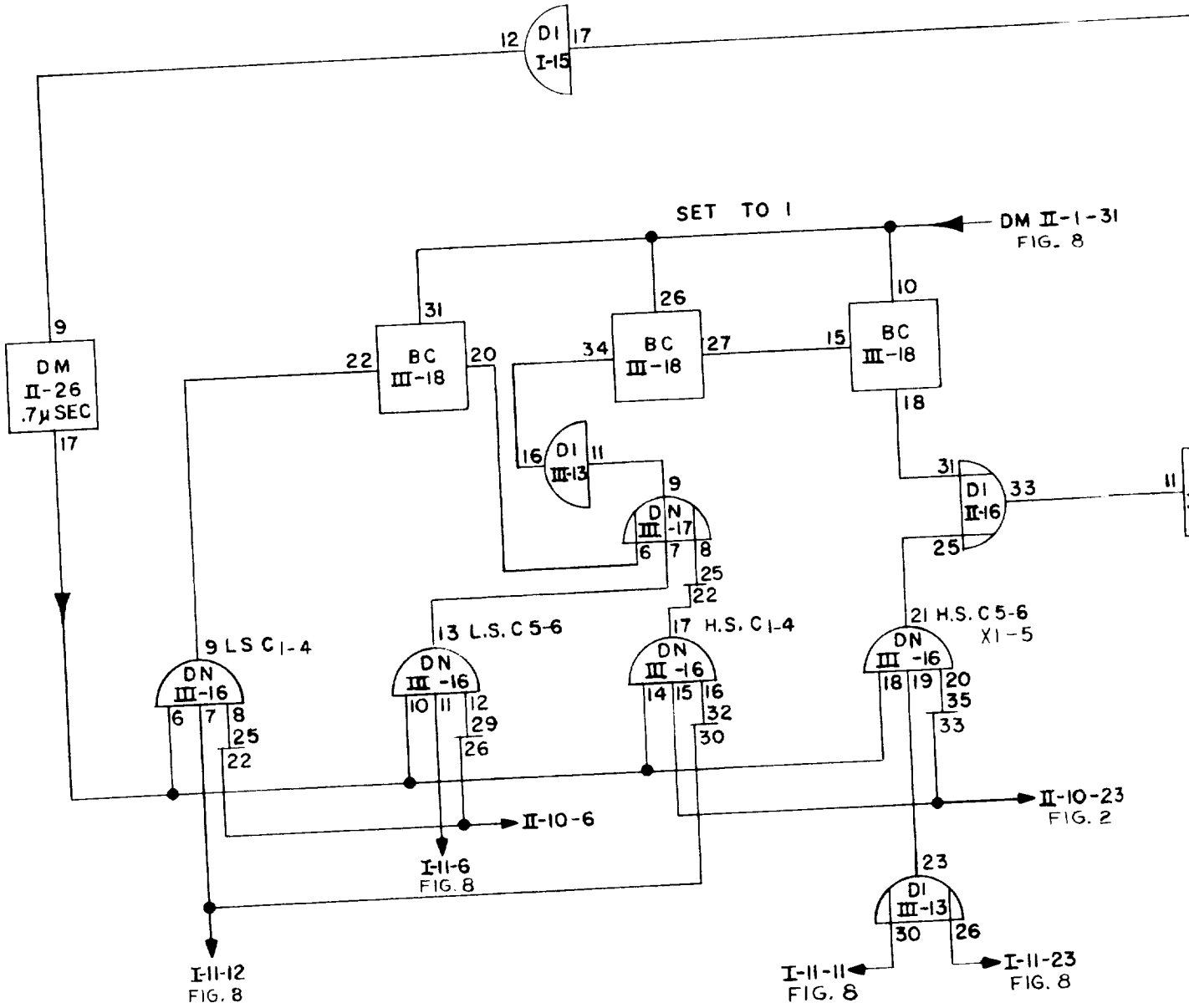

INPUTS FROM FIG. 6
II-13-9
II-14-9
f(0) f(8)
II-13-13
II-14-13
f(1) f(9)
II-13-17
II-14-17
f(2) f(10)
II-15-13
f(15)
II-15-17
f(14)
f(4)
D1 I-19
D1 I-20
FIG. 6 II-10-16
C(0) STROBE DELAYED
f(0,8) C(0)
f(1,9) C(0)
f(2,10) C(0)
f(14) C(0)
#1 STROBE
f(1) C(0)
f(2,10) C(1)
FROM I-15-23 L.S. f(0) C(8) FIG. 5
D1 I-12
READ C5,6 I-8-22 FIG. 8
TO RESET FLAG DECADE C, P3
H.S. f(0) C(0) II-10-27
L.S. f(0) C(14) II-17-27
L.S. f(1) C(10) I 17-23
FIG. 5 I-17-16 L.S. f(0) C(3)
DN I-18
DN I-14
PRINT DIGITAL PRINTER
I-8-17,19
RESET REGISTER FIG. 8
C, P7

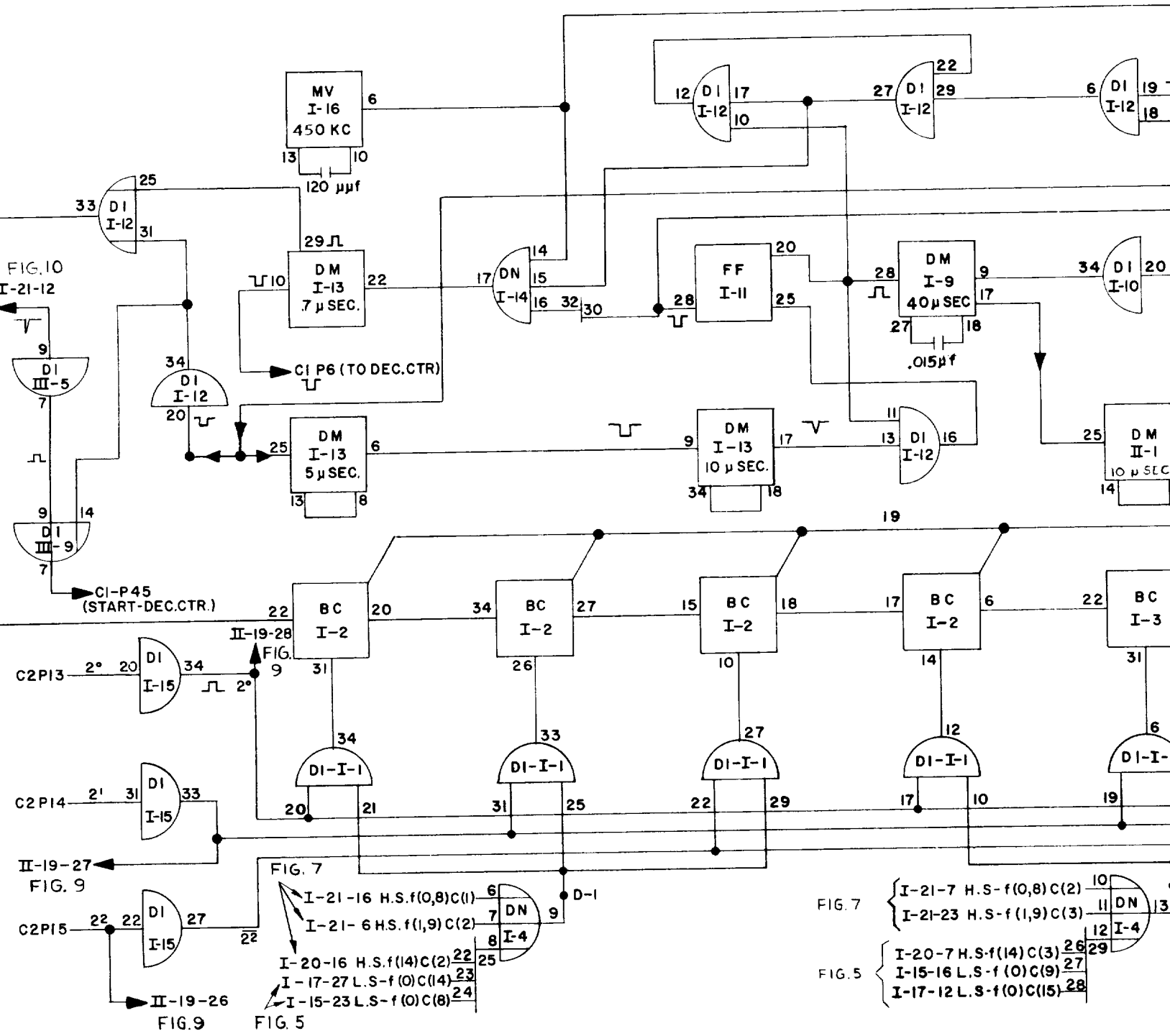
AMMER

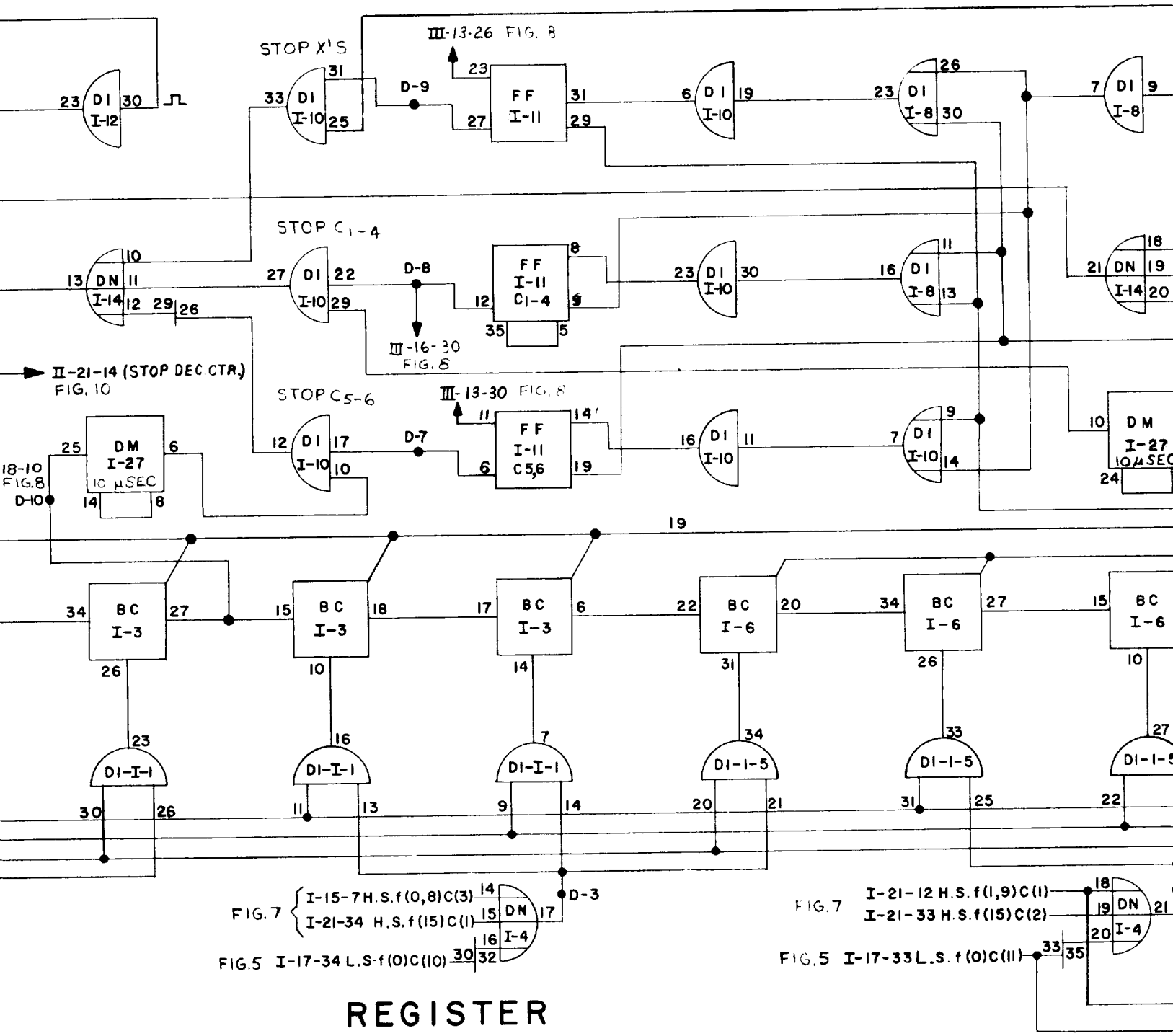


SET
ECIMAL
OUNTER

S-51 FIGURE 7


12
DI
I-15
17
SET TO 1
DM II-1-31
FIG. 8
9
DM
II-26
.7μ SEC
17
31
BC
III-18
22
20
26
BC
III-18
34
27
10
BC
III-18
15
18
16
DI
III-13
11
9
DN
III-17
6
7
8
25
22
31
DI
II-16
33
11
25
9 LS C1-4
DN
III-16
6
7
8
25
22
13 L.S. C 5-6
DN
III-16
10
11
12
29
26
17 H.S. C1-4
DN
III-16
14
15
16
32
30
21 H.S. C 5-6
XI-5
DN
III-16
18
19
20
35
33
II-10-6
I-11-6
FIG. 8
II-10-23
FIG. 2
I-11-12
FIG. 8
23
DI
III-13
30
26
I-11-11
FIG. 8
I-11-23
FIG. 8


MV I-16 450 KC
120 μμf
DM I-13 .7 μ SEC.
DN I-14
FF I-11
DM I-9 40 μ SEC
.015μf
DM I-13 5 μ SEC.
DM I-13 10 μ SEC.
DM II-1 10 μ SEC
CI P6 (TO DEC.CTR)
CI-P45 (START-DEC.CTR.)
BC I-2
BC I-3
DI-I-1
DN I-4
C2P13
C2P14
C2P15
II-19-28
II-19-27
II-19-26
FIG. 9
FIG. 10
I-21-12
FIG. 7
I-21-16 H.S.f(0,8)C(1)
I-21- 6 H.S.f(1,9)C(2)
I-20-16 H.S.f(14)C(2)
I-17-27 L.S-f(0)C(14)
I-15-23 L.S-f(0)C(8)
D-1
I-21-7 H.S-f(0,8)C(2)
I-21-23 H.S-f(1,9)C(3)
FIG. 5
I-20-7 H.S-f(14)C(3)
I-15-16 L.S-f(0)C(9)
I-17-12 L.S-f(0)C(15)


STOP X'S
III-13-26 FIG. 8
D-9
FF I-11
D I I-12
D I I-10
D I I-8
D I I-10
D I I-8
STOP C1-4
D-8
FF I-11 C1-4
DN I-14
D I I-10
D I I-10
D I I-8
DN I-14
III-16-30 FIG. 8
II-21-14 (STOP DEC. CTR.) FIG. 10
STOP C5-6
III-13-30 FIG. 8
D-7
FF I-11 C5,6
DM I-27 10 μSEC
D I I-10
D I I-10
D I I-10
DM I-27 10 μSEC
18-10 FIG. 8
D-10
19
BC I-3
BC I-3
BC I-3
BC I-6
BC I-6
BC I-6
DI-I-1
DI-I-1
DI-I-1
DI-I-5
DI-I-5
DI-I-5
FIG. 7 I-15-7 H.S.f(0,8)C(3)
I-21-34 H.S.f(15)C(1)
DN I-4
D-3
FIG. 5 I-17-34 L.S-f(0)C(10)
FIG. 7 I-21-12 H.S.f(1,9)C(1)
I-21-33 H.S.f(15)C(2)
DN I-4
FIG. 5 I-17-33 L.S.f(0)C(11)

REGISTER

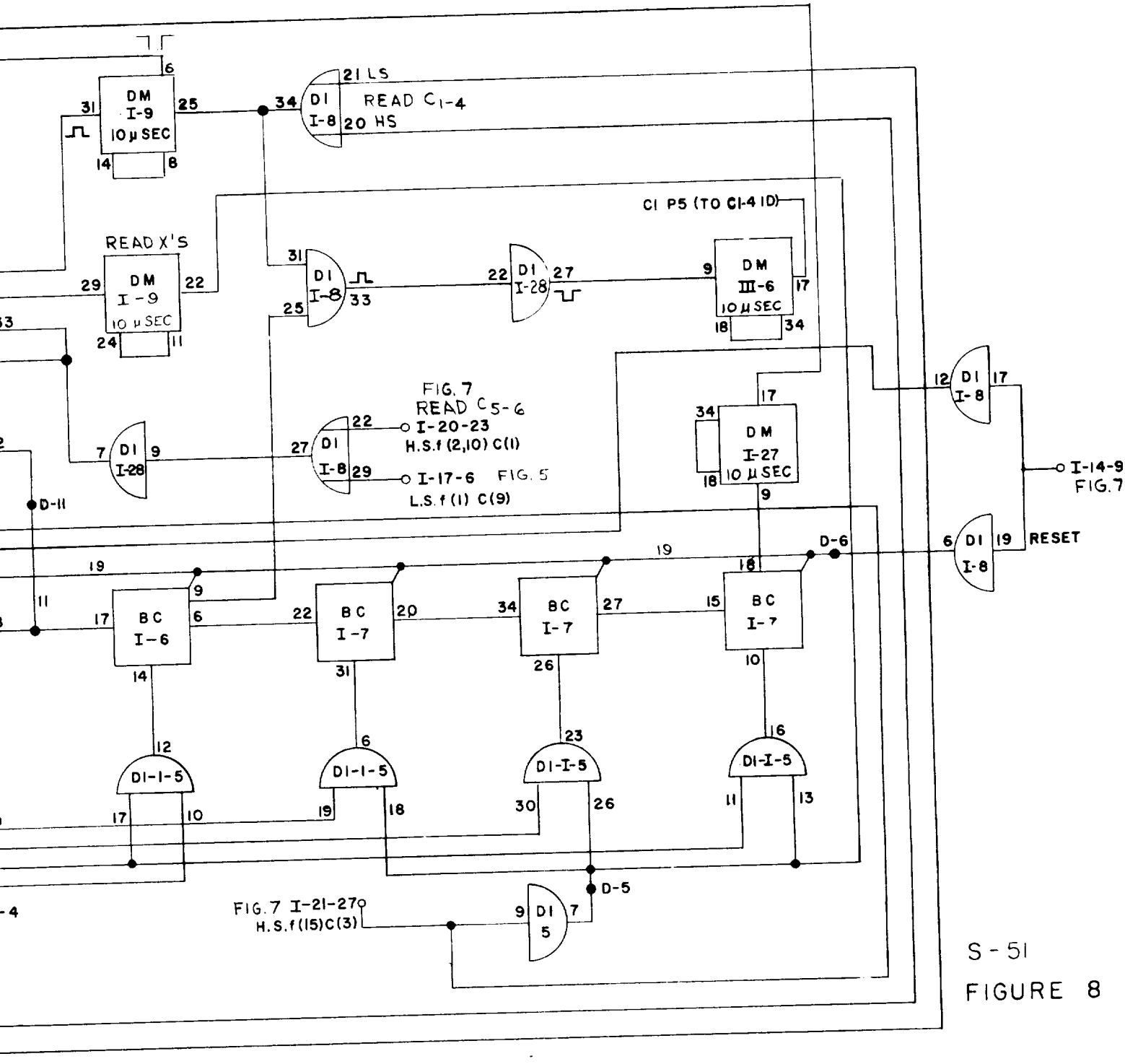

DM I-9 10 μSEC
DI I-8 READ C1-4 20 HS 21 LS
READ X'S
DM I-9 10 μSEC
DI I-8
DI I-28
DM III-6 10 μSEC
CI P5 (TO CI-4 ID)
FIG. 7 READ C5-6
I-20-23 H.S.f (2,10) C(1)
I-17-6 FIG. 5 L.S.f (1) C(9)
DM I-27 10 μSEC
I-14-9 FIG. 7
RESET
D-11
D-6
D-5
BC I-6
BC I-7
BC I-7
BC I-7
DI-1-5
DI-1-5
DI-I-5
DI-I-5
FIG. 7 I-21-27 H.S.f (15) C(3)
DI 5

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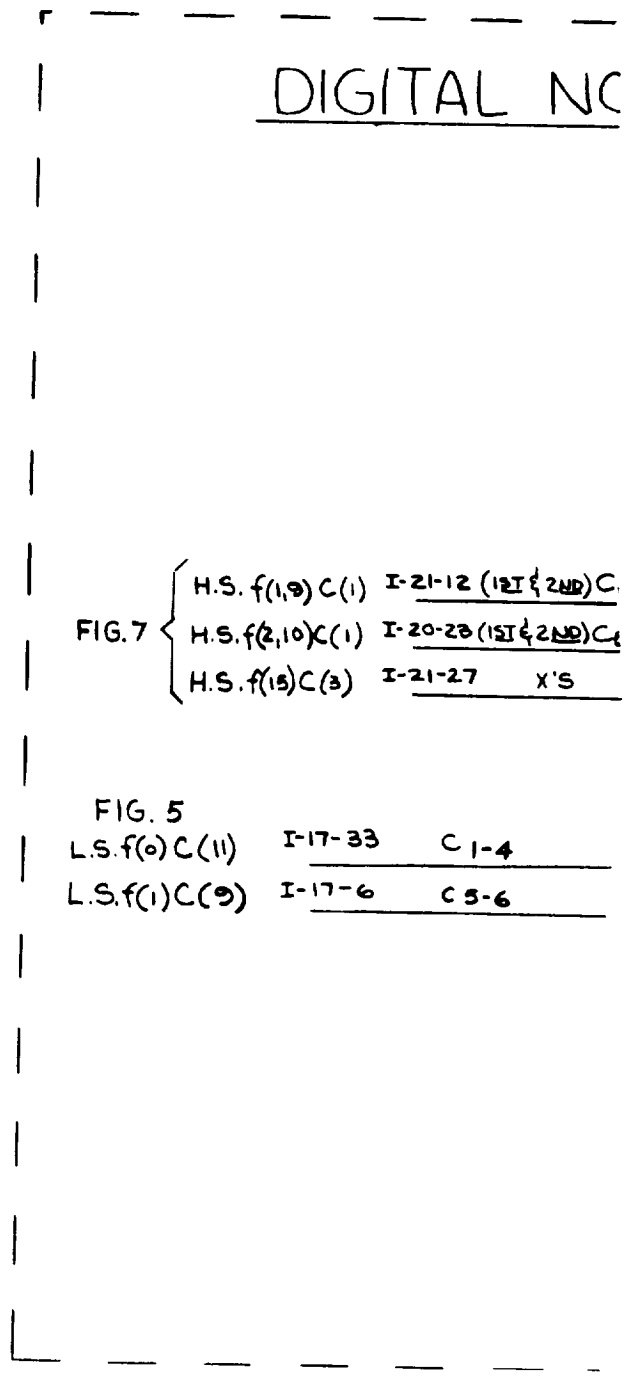
FIGURE 8

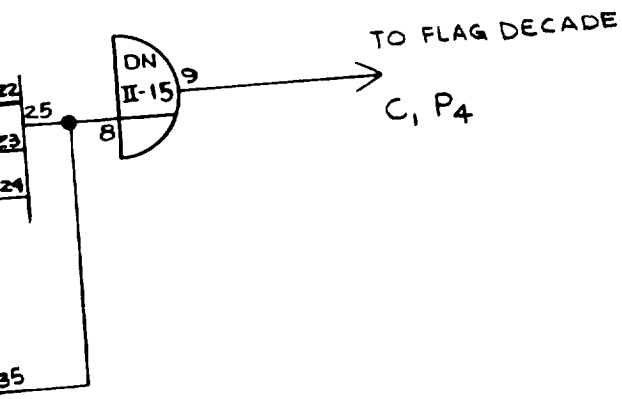

DIGITAL NC
FIG. 7
H.S. f(1,9) C(1) I-21-12 (1ST & 2ND) C
H.S. f(2,10) C(1) I-20-28 (1ST & 2ND) C
H.S. f(15) C(3) I-21-27 X'S
FIG. 5
L.S. f(0) C(11) I-17-33 C 1-4
L.S. f(1) C(9) I-17-6 C 5-6

DENTIFIER

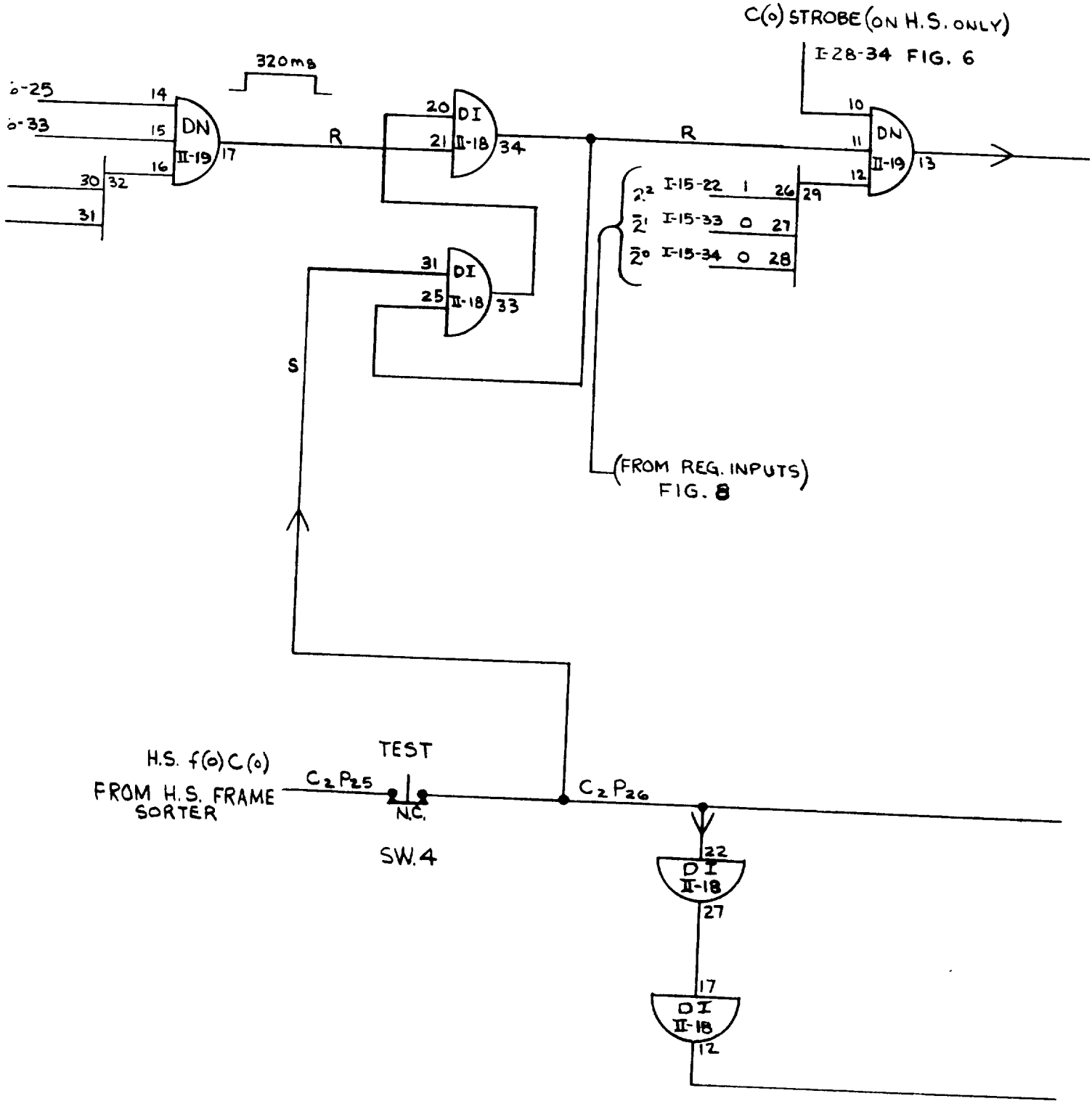
FROM SIMULATOR FIG. 20

II-6-18

II-6-6



SEQUENCE COUNTER CONTR



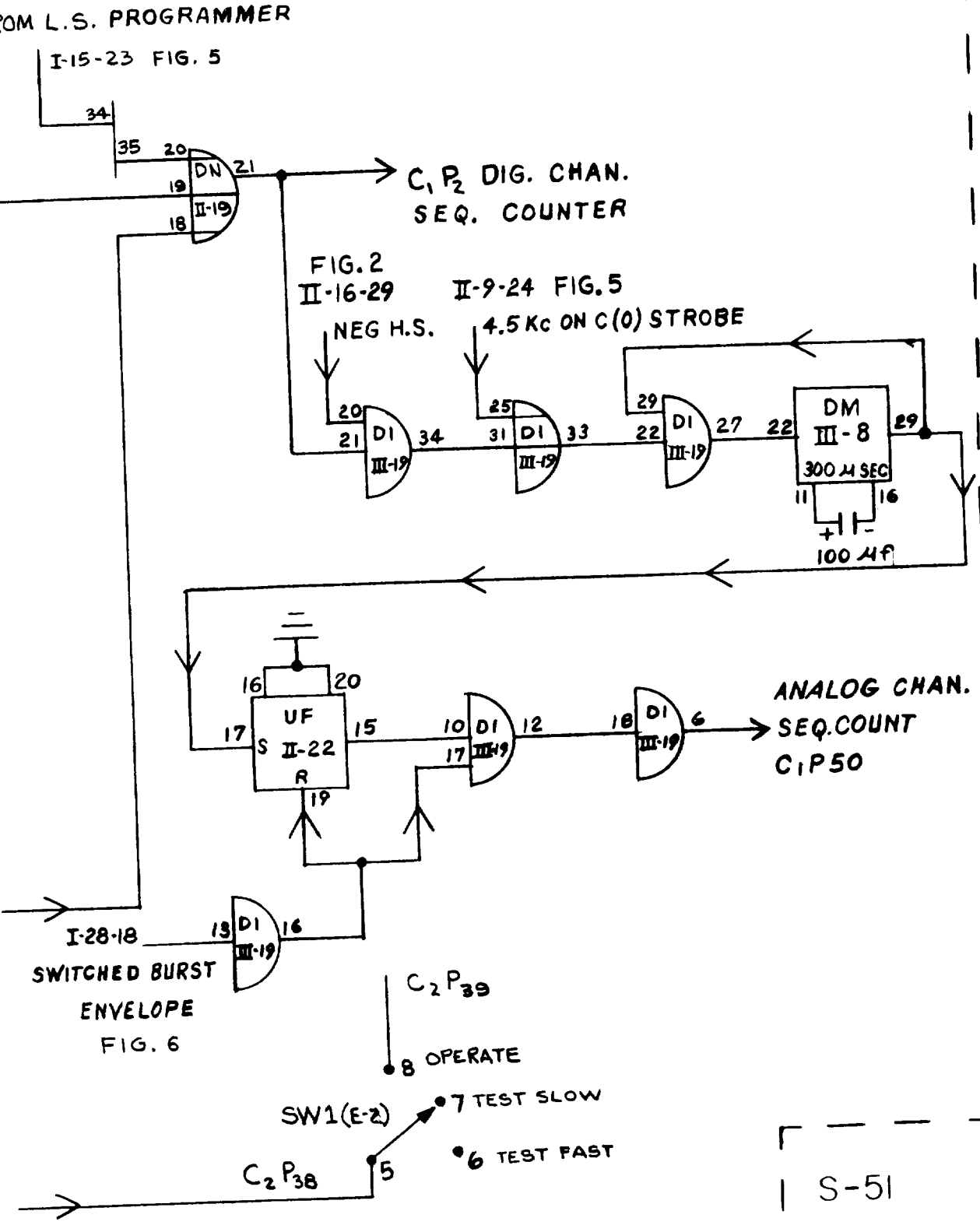

OM L.S. PROGRAMMER
I-15-23 FIG. 5
34
35
20
DN
21
19
II-19
18
C1 P2 DIG. CHAN.
SEQ. COUNTER
FIG. 2
II-16-29
II-9-24 FIG. 5
NEG H.S.
4.5 Kc ON C(0) STROBE
20
21
DI
III-19
34
25
31
DI
III-19
33
29
22
DI
III-19
27
22
DM
III-8
300 μ SEC
29
11
16
+
100 μf
16
20
UF
17
S II-22
R
19
15
10
DI
17
III-19
12
18
DI
III-19
6
ANALOG CHAN.
SEQ.COUNT
C1P50
I-28-18
SWITCHED BURST
ENVELOPE
FIG. 6
13
DI
III-19
16
C2 P39
8 OPERATE
SW1(E-2)
7 TEST SLOW
6 TEST FAST
C2 P38
5

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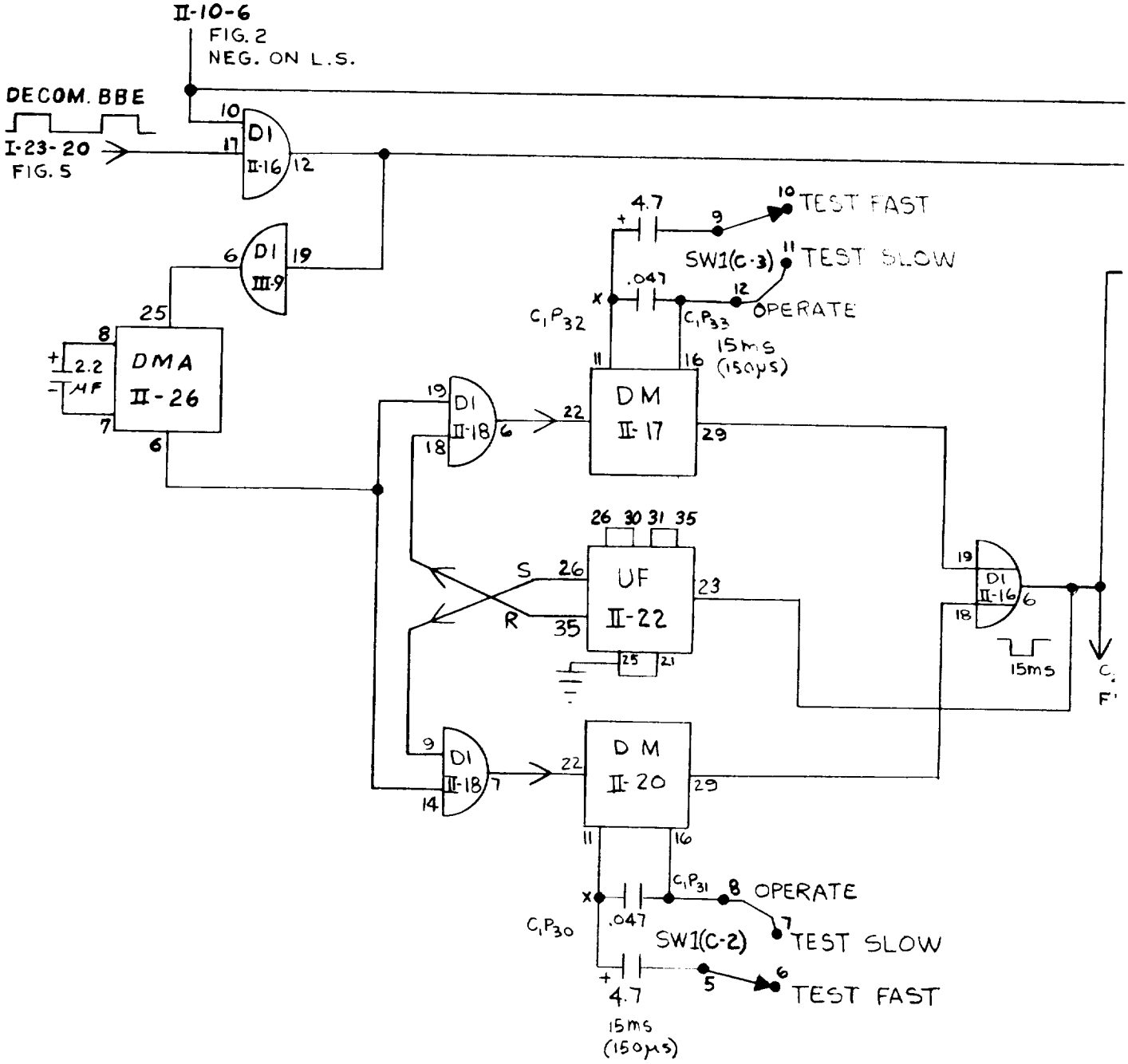
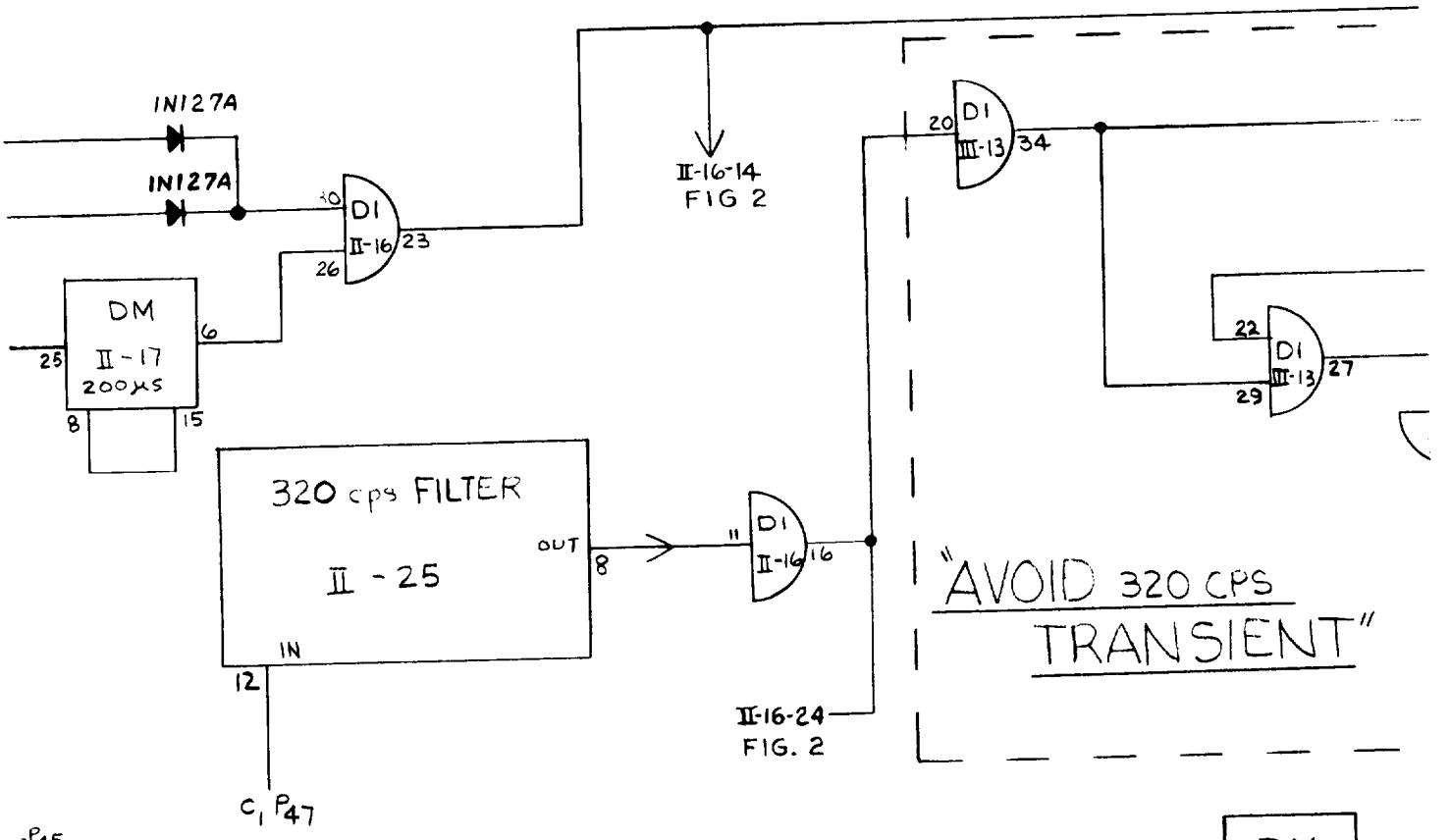
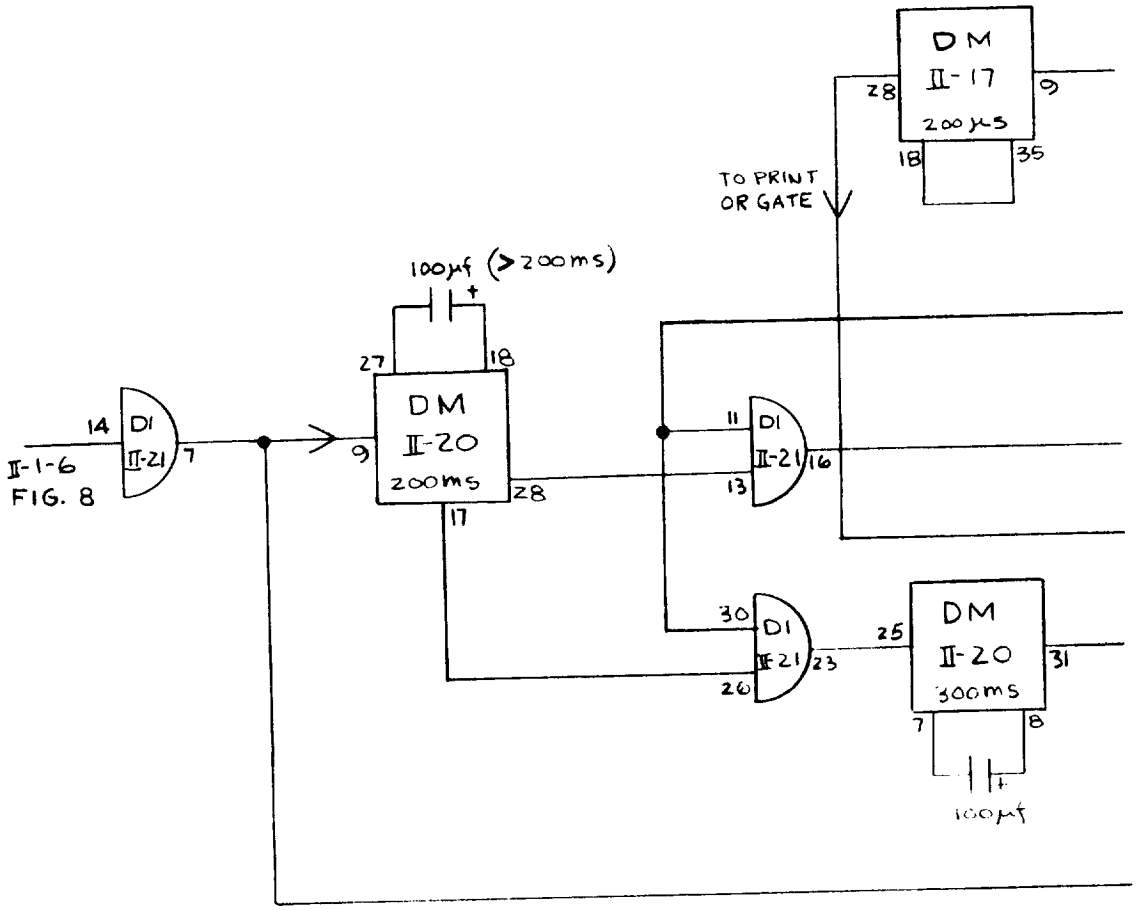
FIGURE 9


II-10-6
FIG. 2
NEG. ON L.S.
DECOM. BBE
I-23-20
FIG. 5
D1
II-16
D1
III-9
DMA
II-26
2.2 MF
4.7
TEST FAST
SW1(C-3)
TEST SLOW
.047
OPERATE
C1P32
C1P33
15ms
(150μs)
DM
II-17
D1
II-18
UF
II-22
S
R
DM
II-20
C1P31
C1P30
SW1(C-2)
TEST SLOW
TEST FAST
4.7
15ms
(150μs)
15ms

END OF HIGH OR LOW SEQUENCES



P45
IG. 2



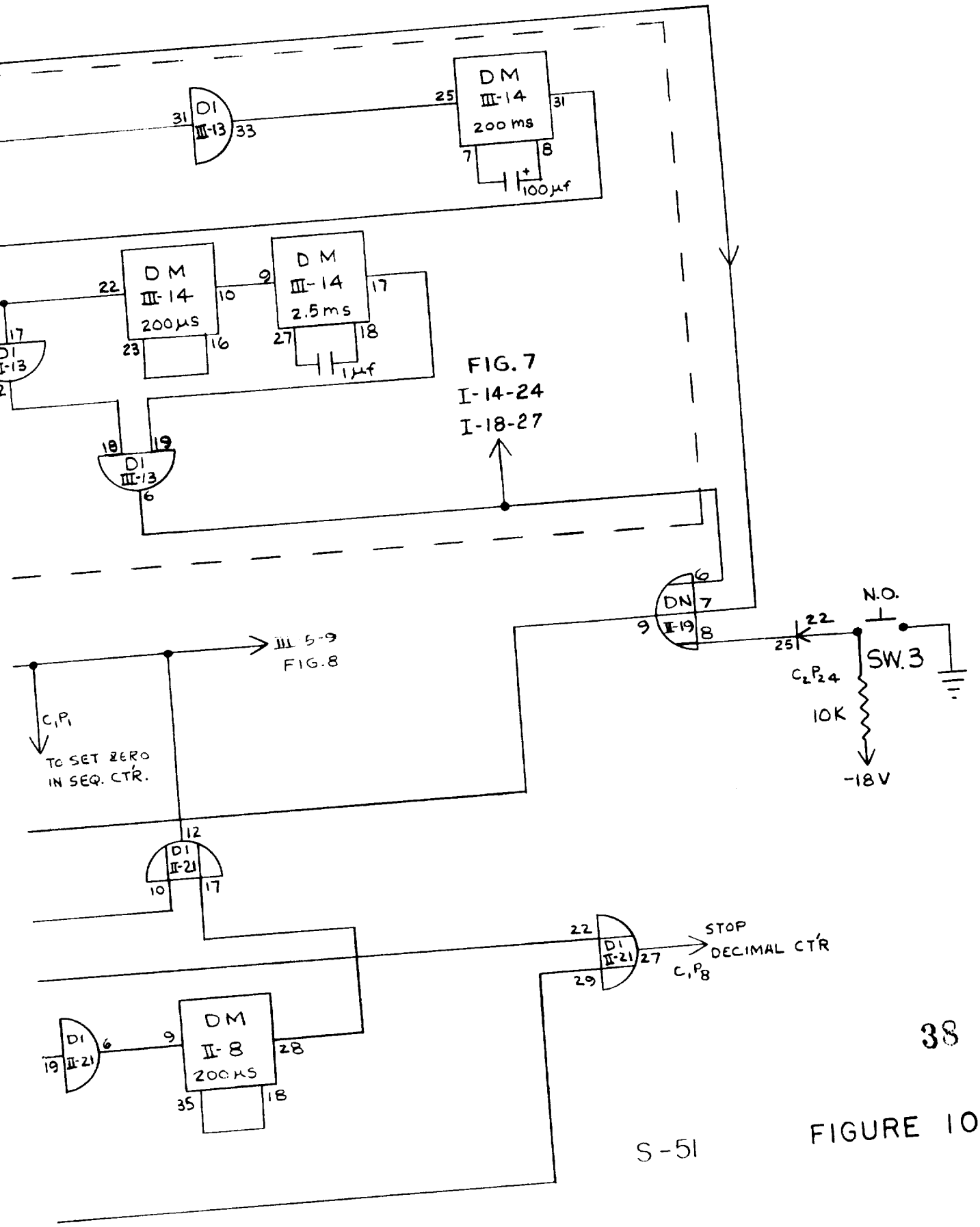


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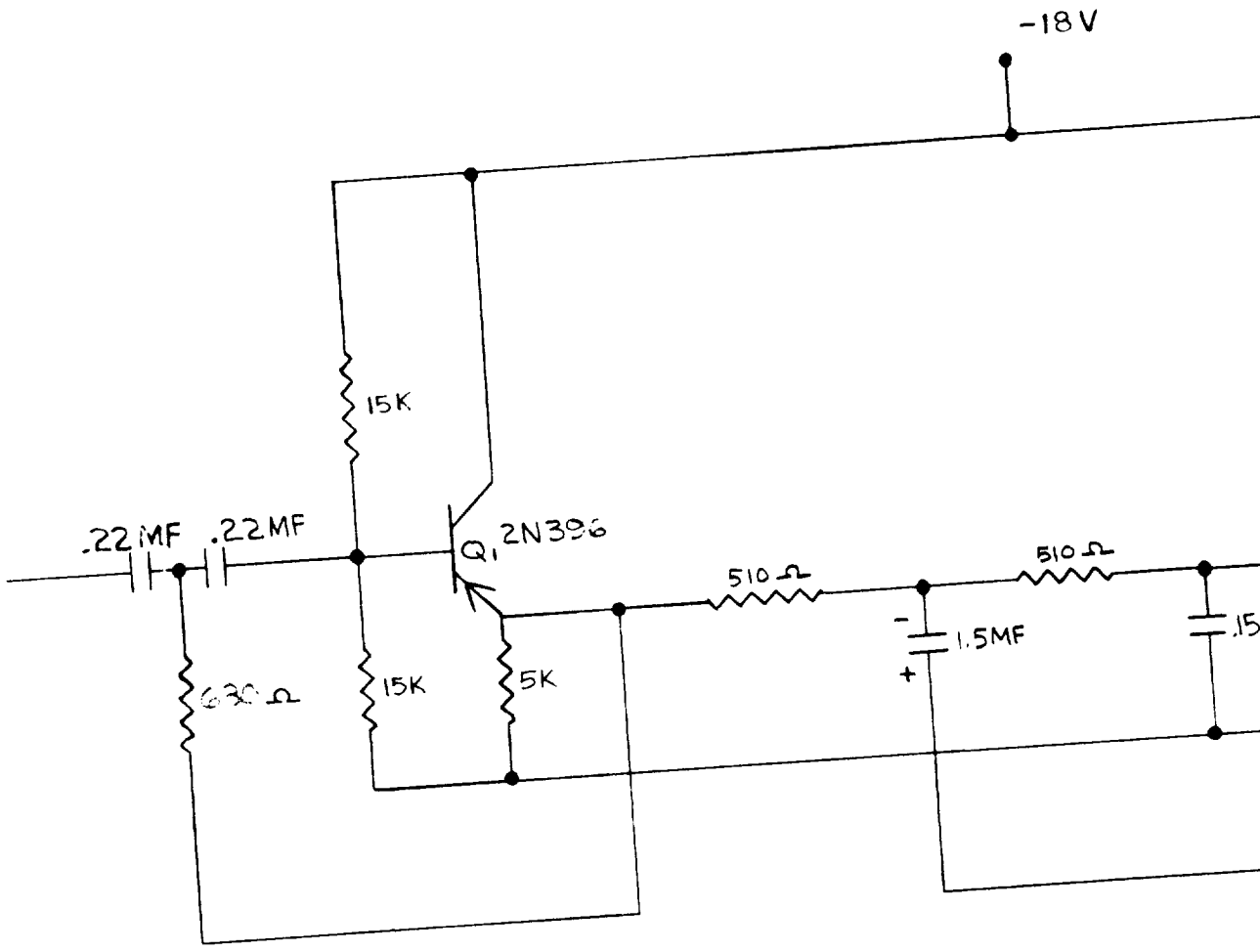
FIGURE 10

320 CPS



BAND PASS FILTER

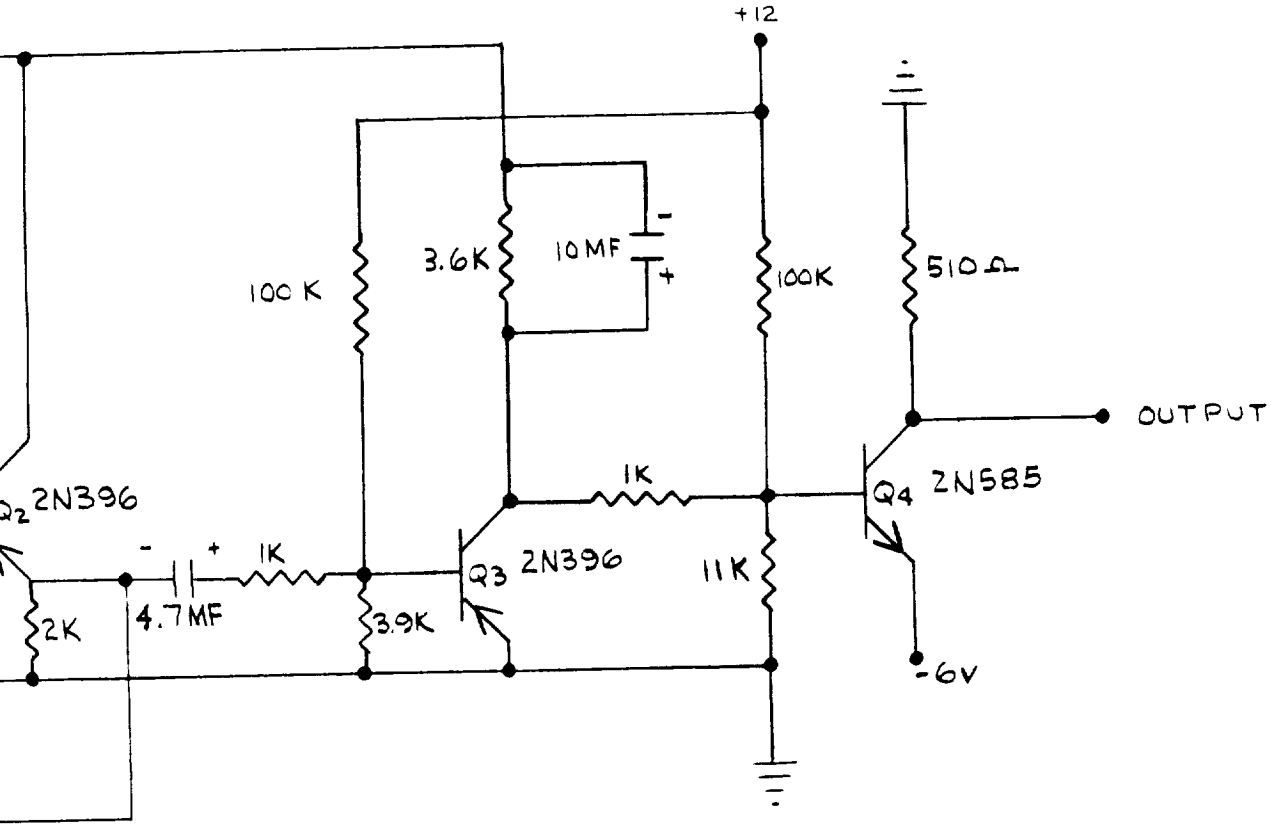


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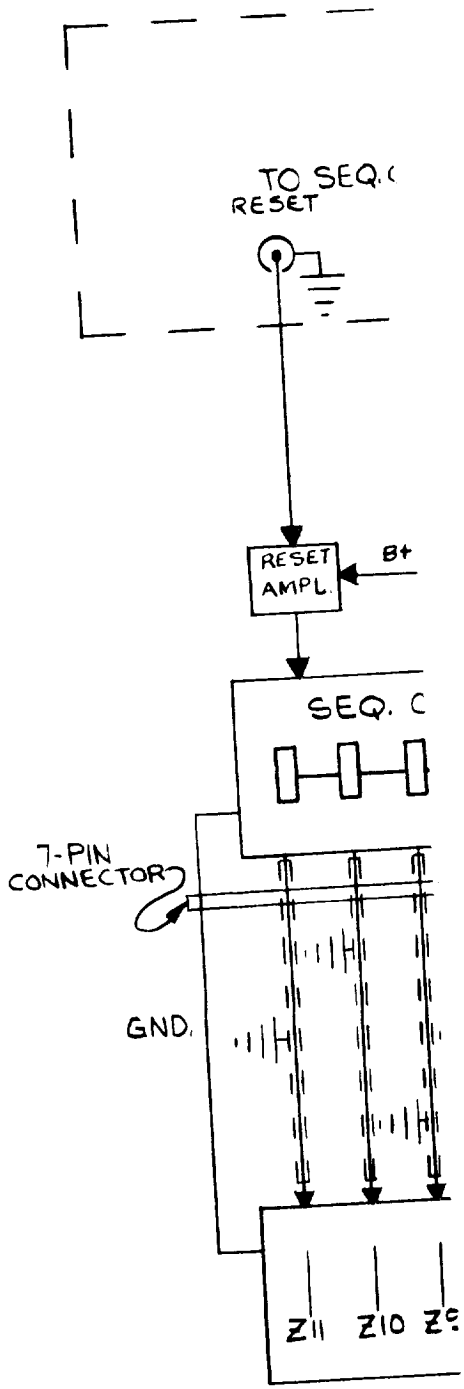
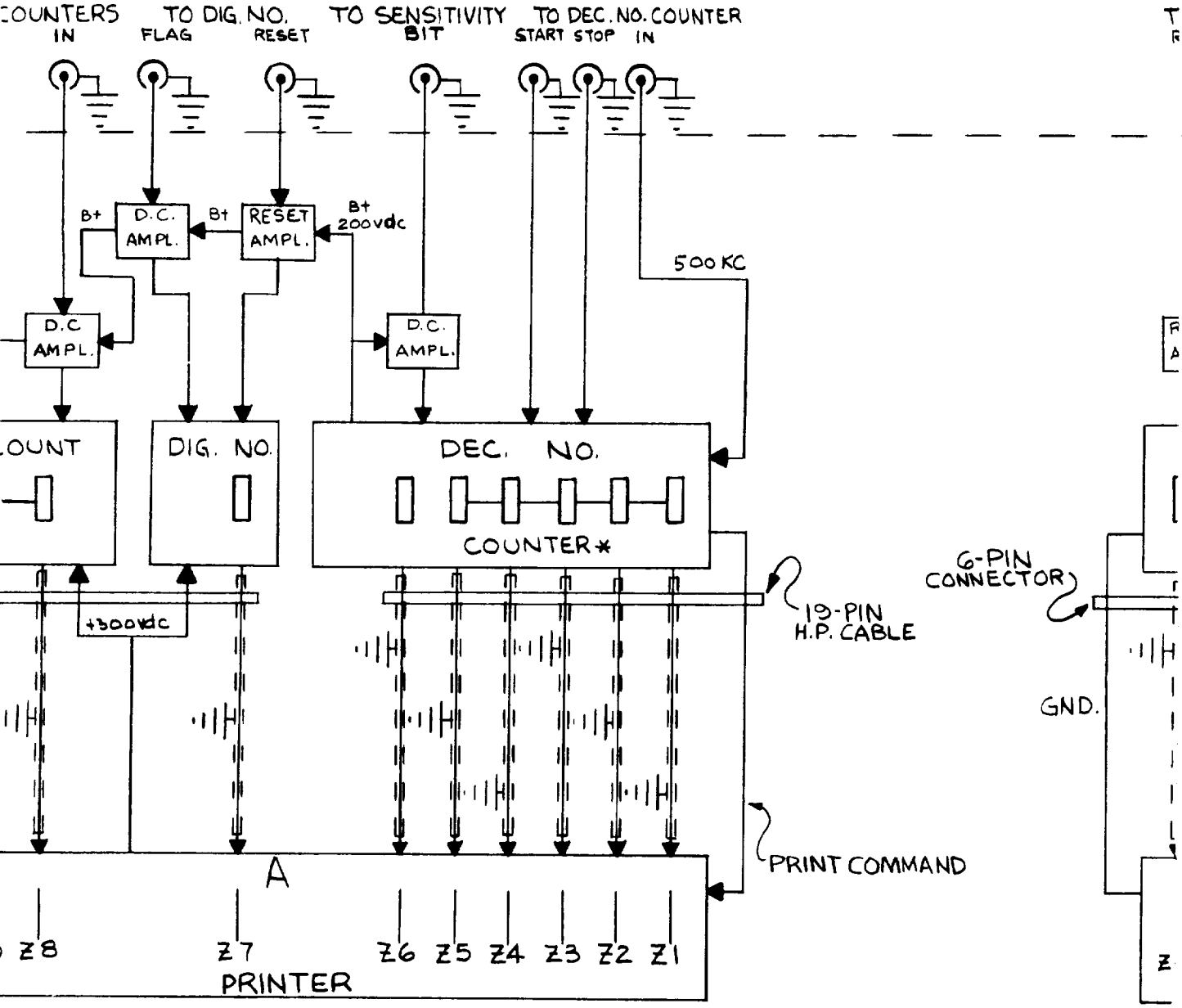
FIGURE 11


TO SEQ.
RESET
RESET AMPL.
B+
SEQ. C
7-PIN CONNECTOR
GND.
Z11
Z10

COUNTER-PRINTER OPERATI

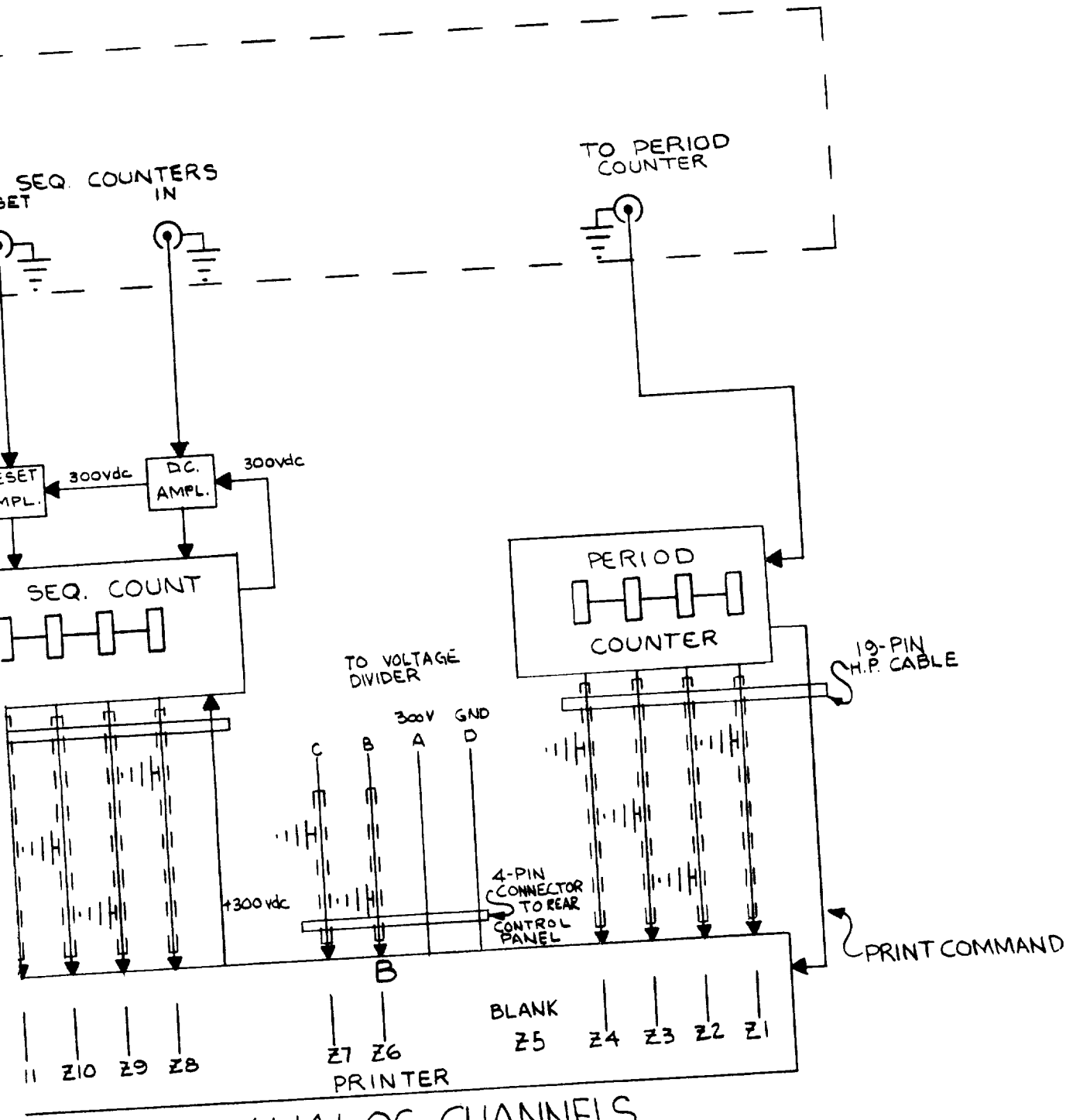
CONTROL PANEL
(REAR)



DIGITAL CHANNELS

* SET COUNTER TO TIME INTERVAL + EXT
USE STANDARD FREQ. CTD. INPUT.

N

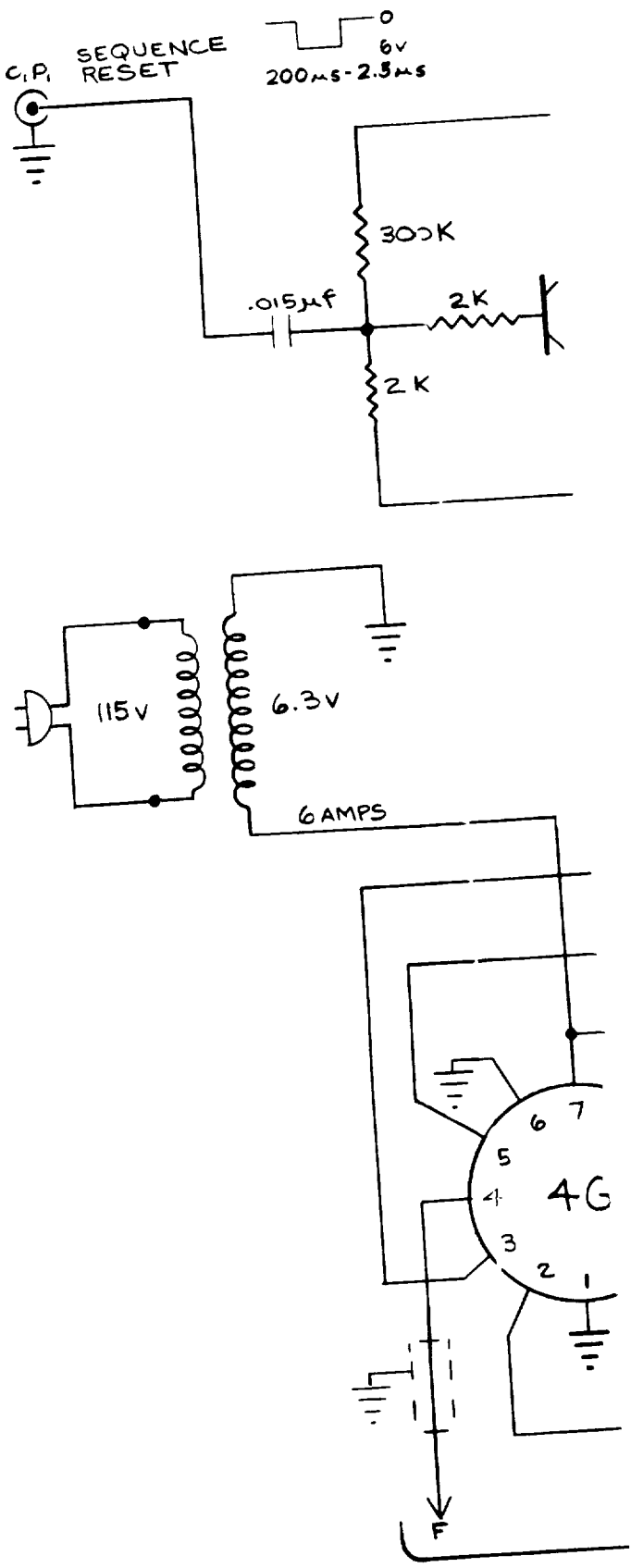


ANALOG CHANNELS

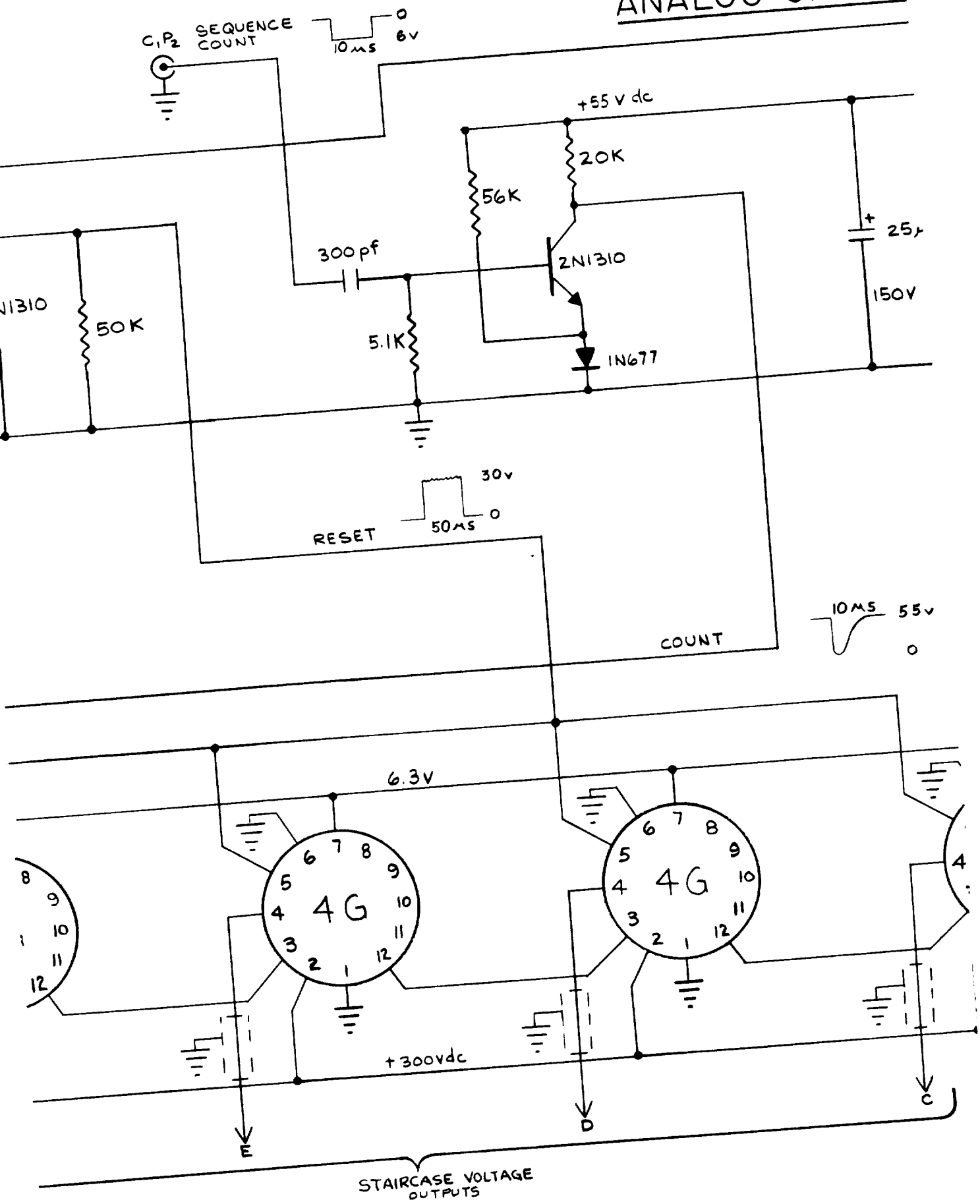
40

ERNAL-

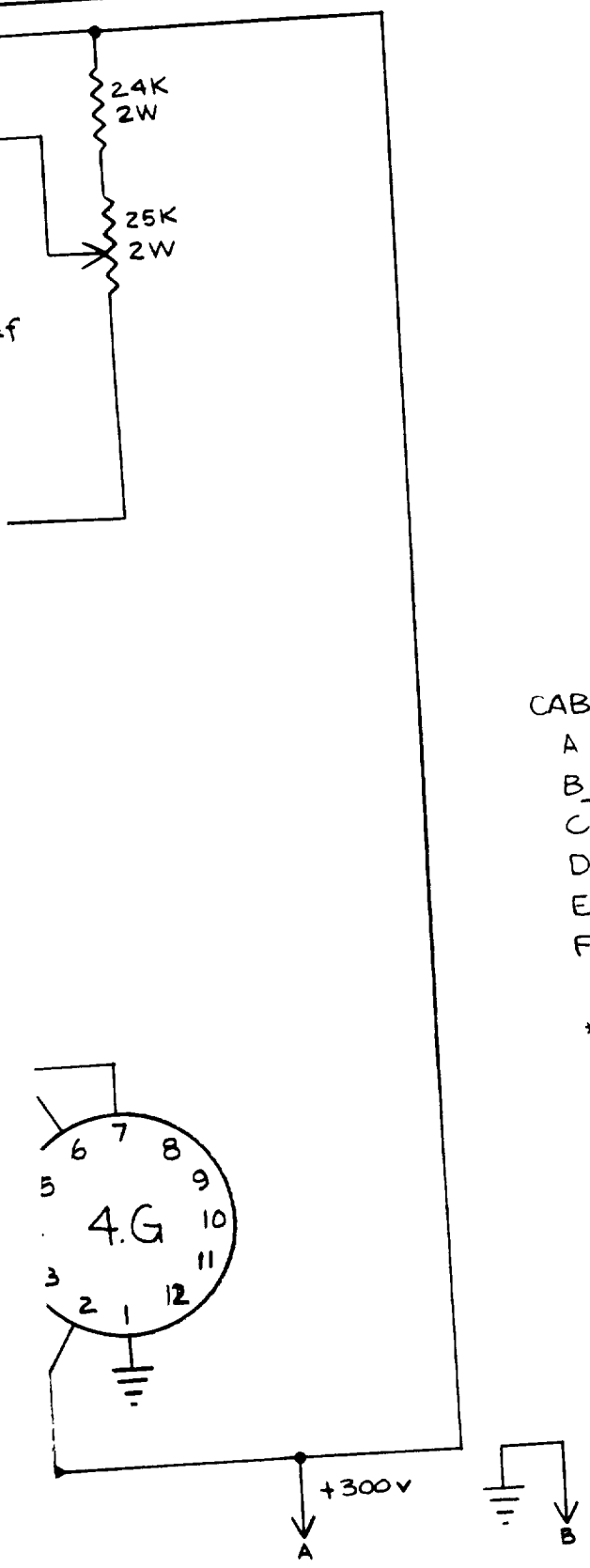
FIGURE 12


C.P.I. SEQUENCE RESET
0
6v
200ms-2.5ms
300K
.015μf
2K
2K
115V
6.3V
6 AMPS
6
7
5
4
3
2
1
4G
F

ANALOG CHANN



EL SEQUENCE COUNTER



CABLE CONNECTIONS

A (+300 v)

B (GND.)

C ---------- Z11

D ---------- Z10

E ---------- Z9

F ---------- Z8

TO PRINTER COMPARATORS PIN *3*

* REMOVE WIRE PREVIOUSLY CONNECTED TO PIN *3.

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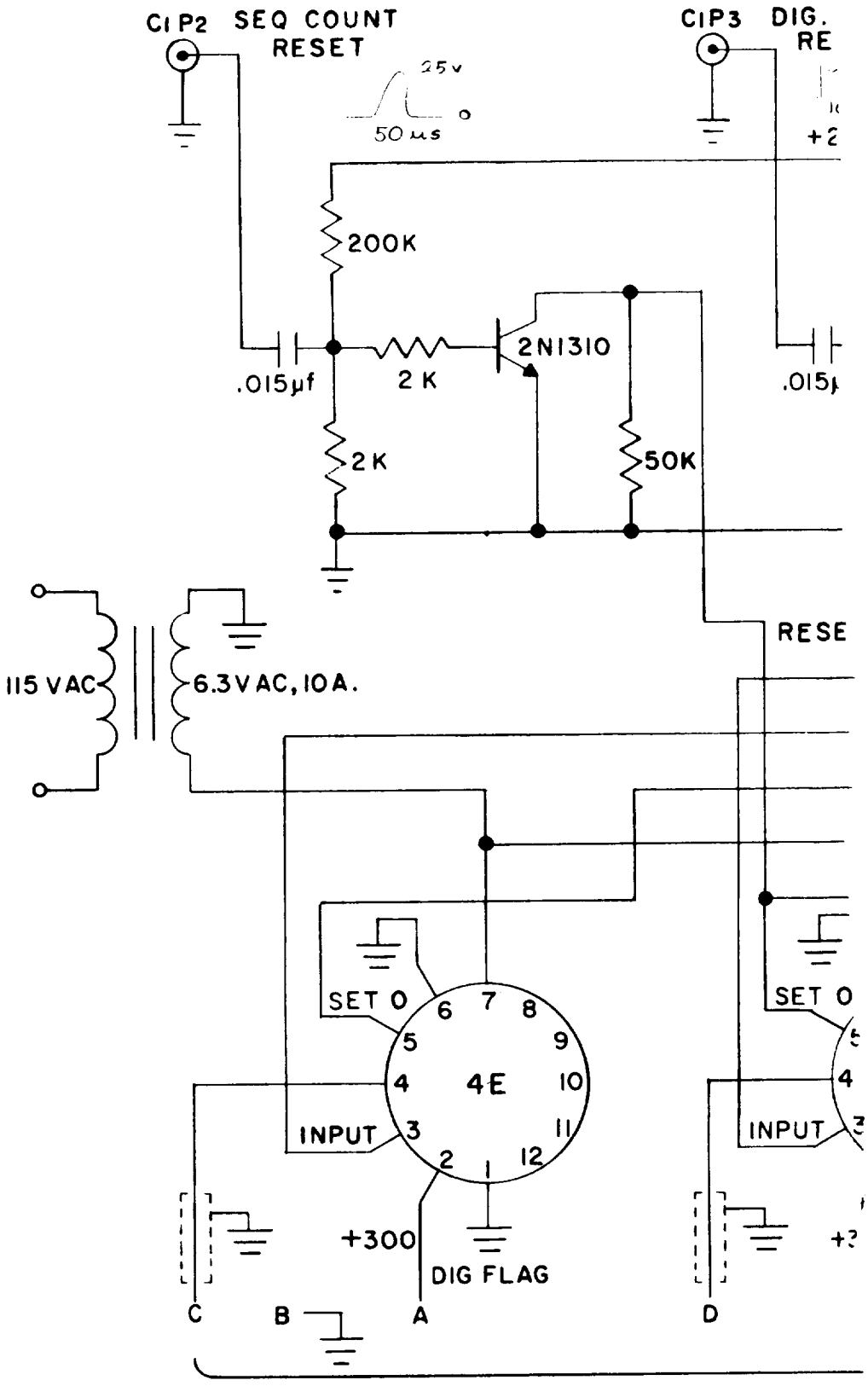
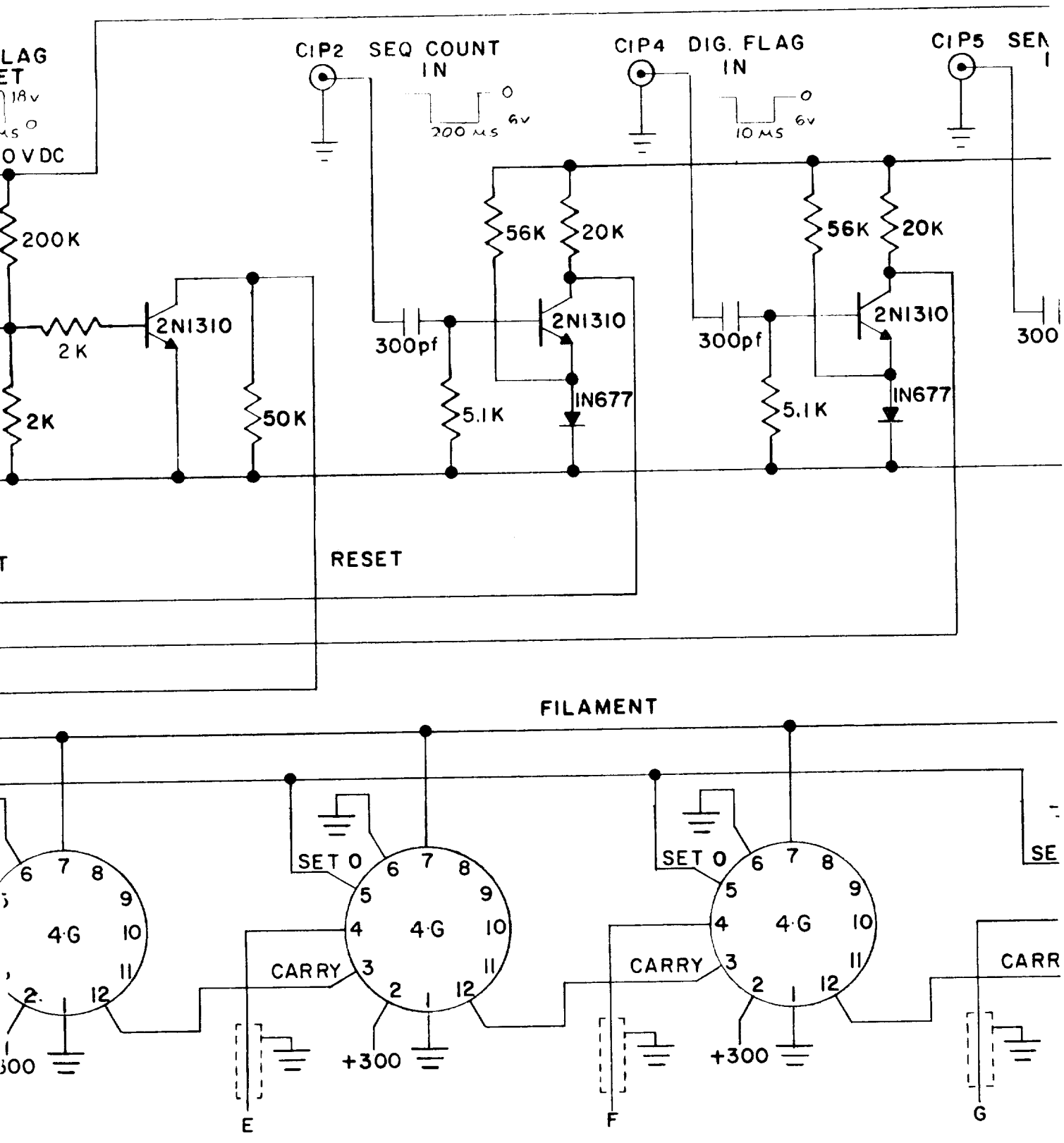
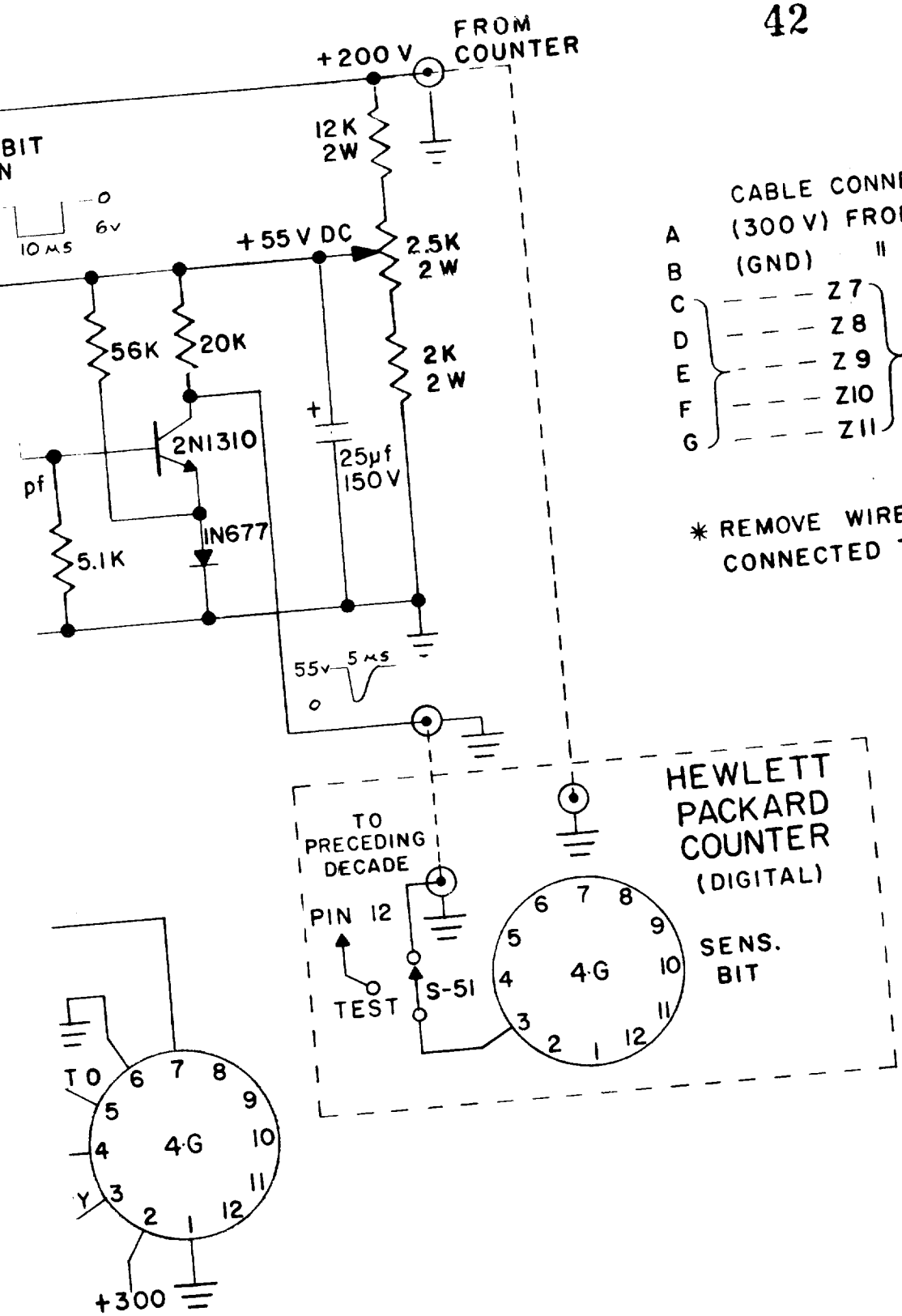
FIGURE 13


C1P2 SEQ COUNT RESET
25v
0
50 μs
C1P3 DIG. RE
+2
200K
.015μf
2 K
2N1310
2K
50K
.015μ
RESE
115 VAC
6.3VAC, 10A.
SET 0
4E
INPUT
+300
DIG FLAG
C
B
A
D
SET 0
INPUT
+?



DIGITAL CHANNEL SEQUENCE C



42

OUNTER AND FLAG

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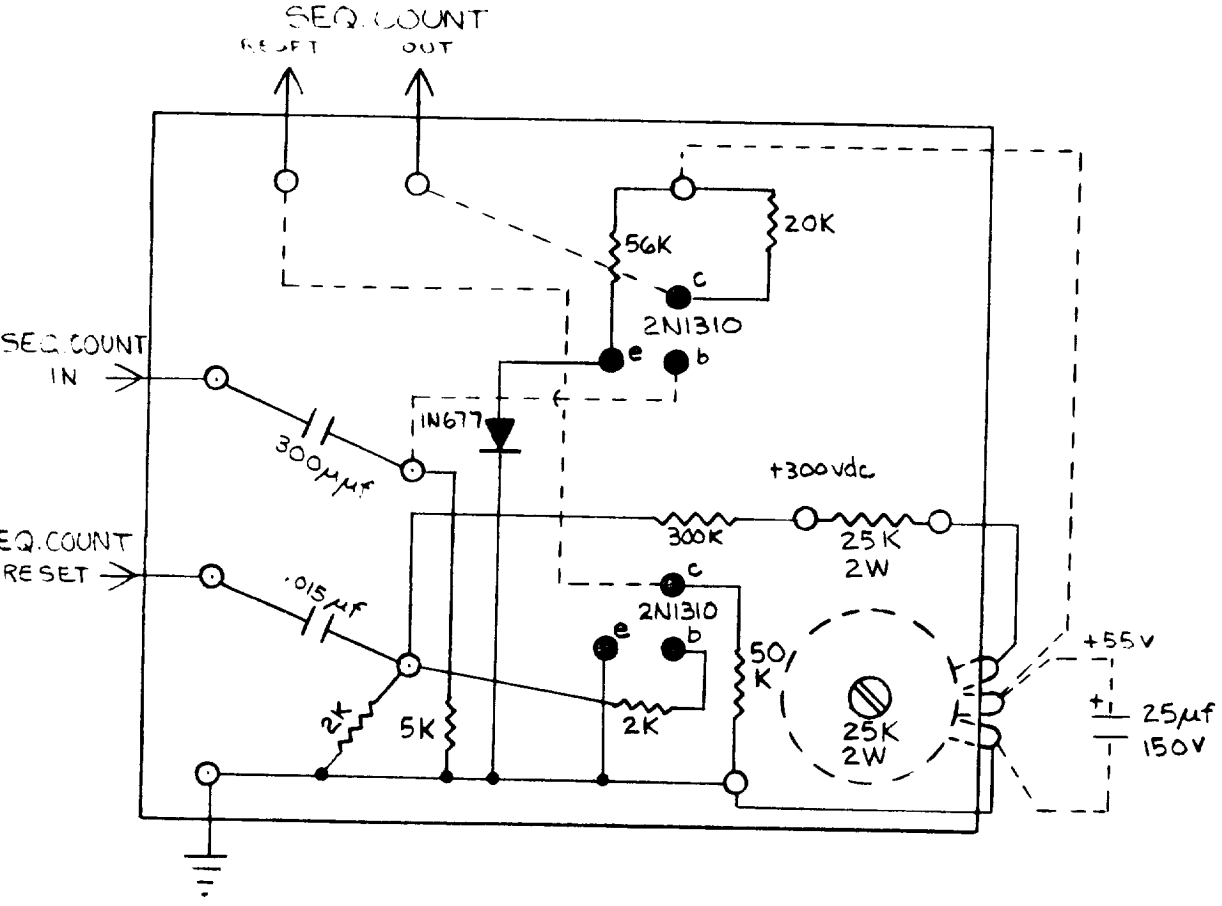
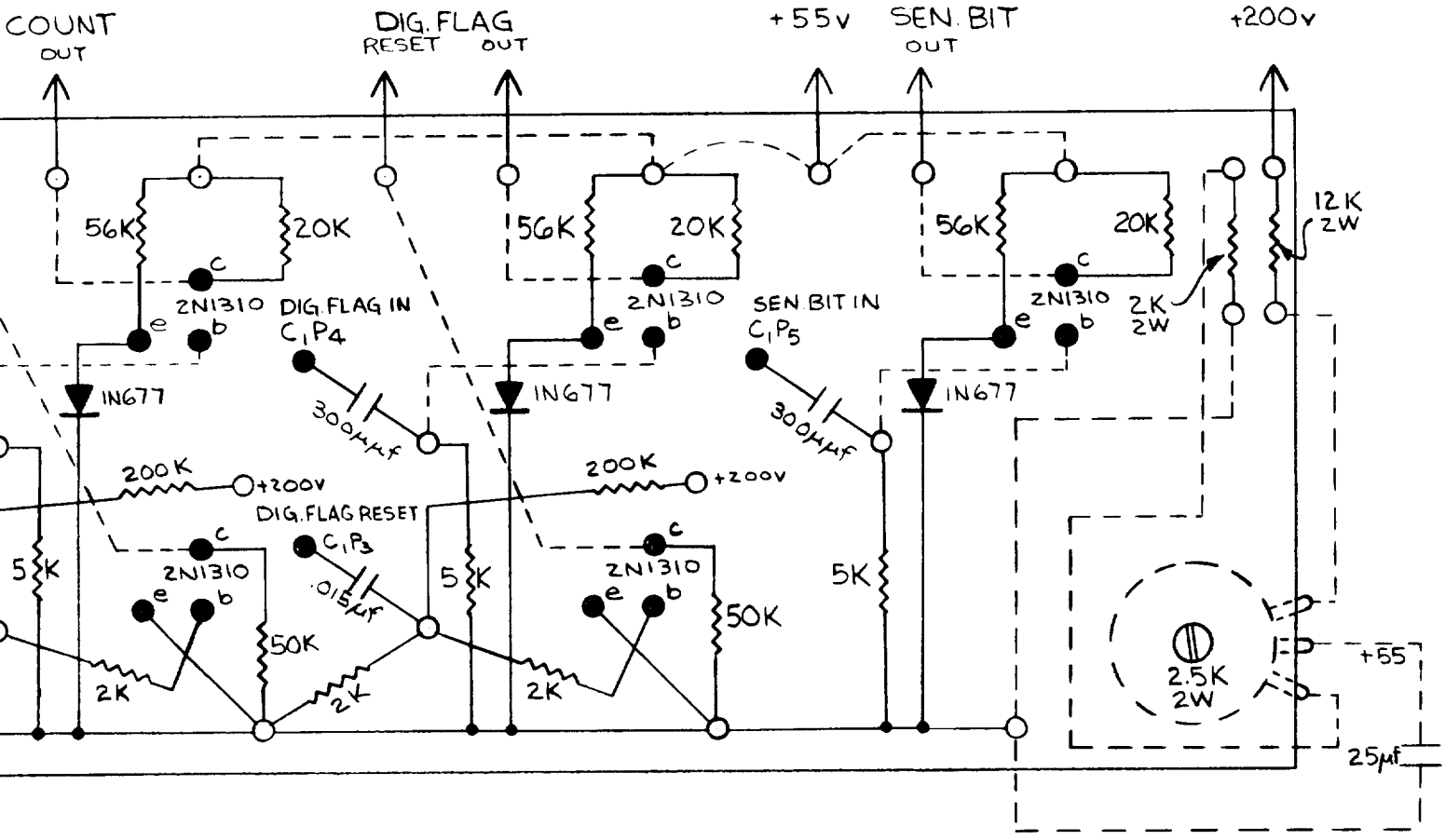
FIGURE 14

DECADE COUNTER INPU

LOCATED ON ANALOG
CHANNEL DECADE CHASSIS



LOCATED ON DIGITAL
CHANNEL DECADE CHASSIS



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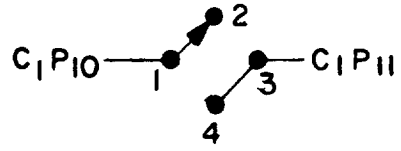
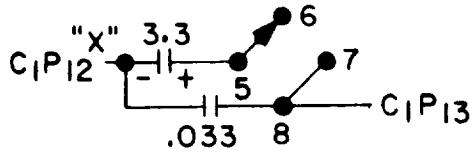
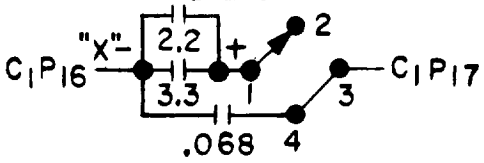
SECT A-1



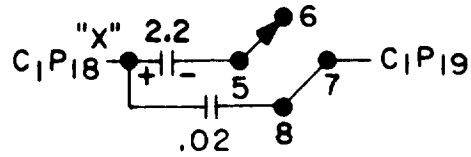
SECT A-2



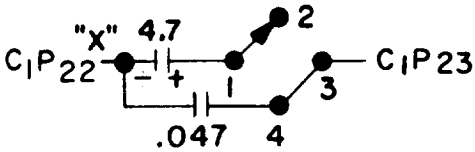
SECT B-1



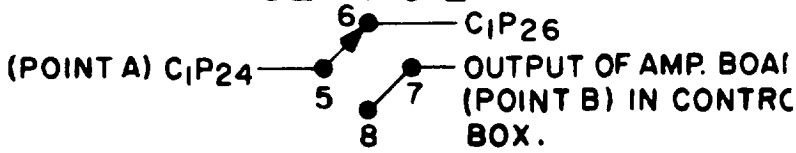
SECT B-2



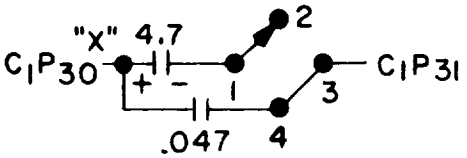
SECT C-1



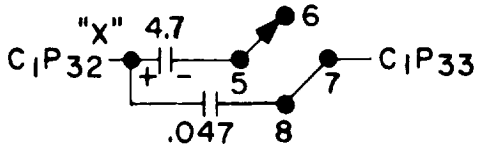
SECT C-2



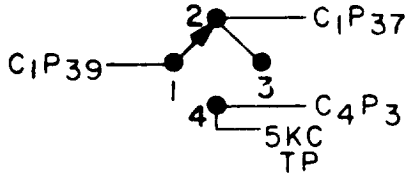
SECT D-1



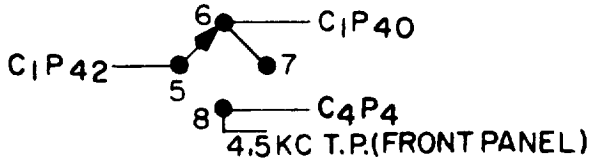
SECT D-2



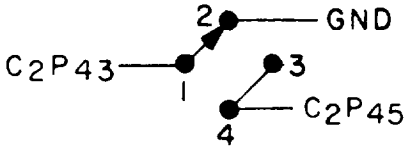
SECT E-1



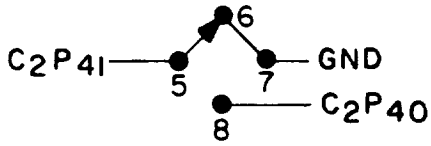
SECT E-2



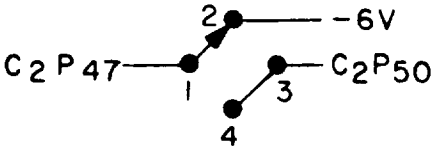
SECT F-1



SECT F-2

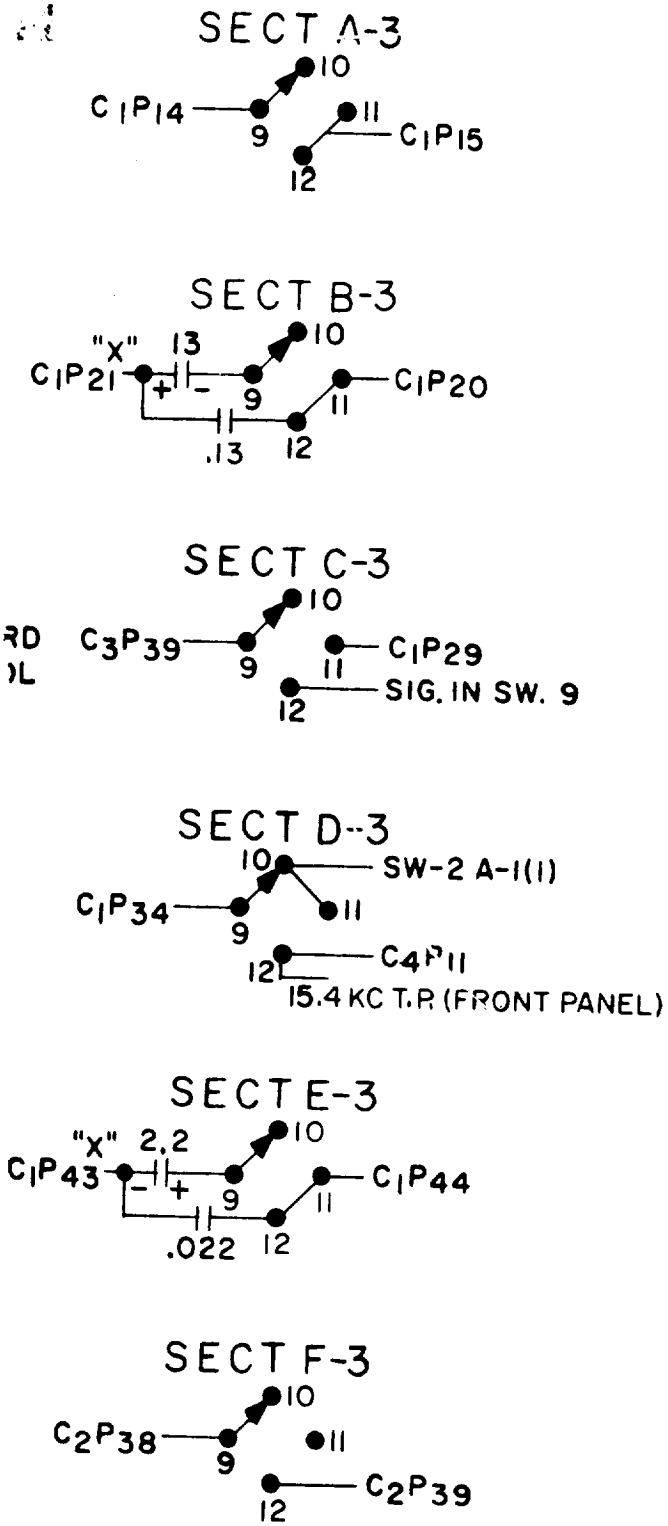


SECT G-1



CONTROL PANEL SW#1

TEST STAND SER #1 ONLY



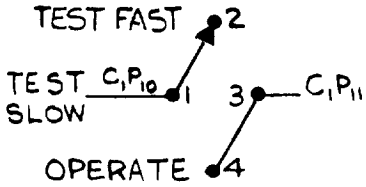
NOTE:
ALL CAPACITOR VALUES
ARE IN μμF

S-51 FIGURE 16-A

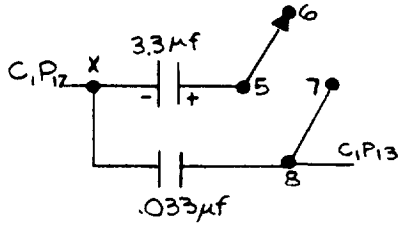
CONTR

TEST ST

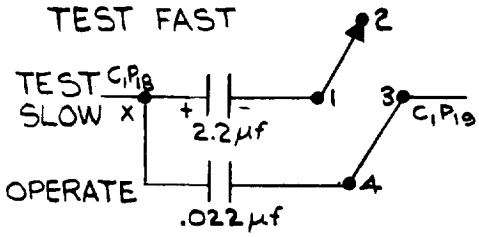
SEC A-1



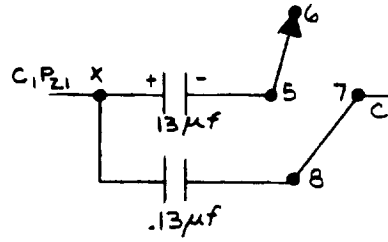
SEC A-2



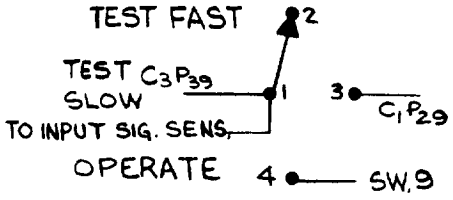
SEC B-1



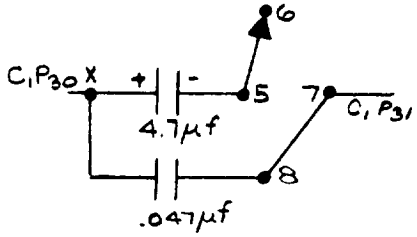
SEC B-2



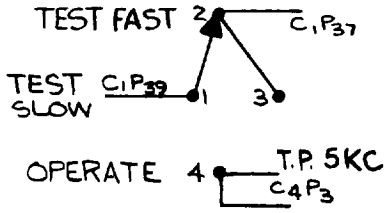
SEC C-1



SEC C-2



SEC D-1



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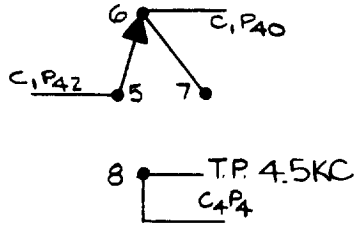
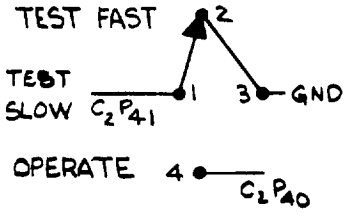
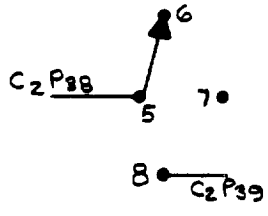


SEC E-1



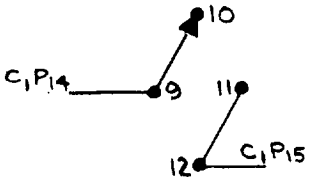
SEC E-2



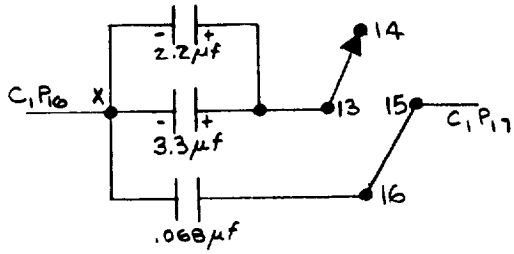
PANEL SW. #1

SER. #2 & 3 ONLY

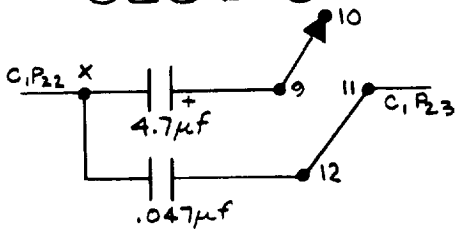
SEC A-3



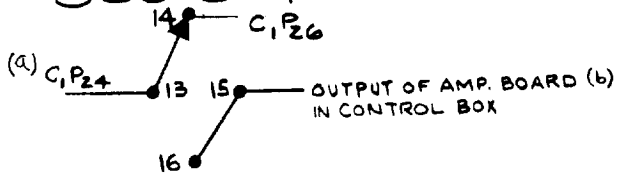
SEC A-4



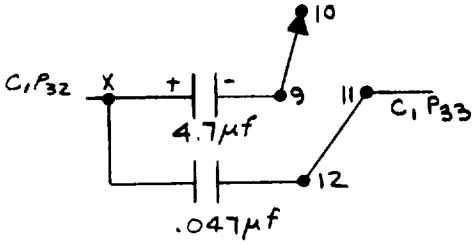
SEC B-3



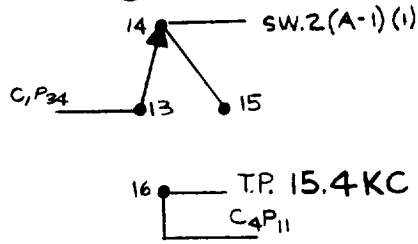
SEC B-4



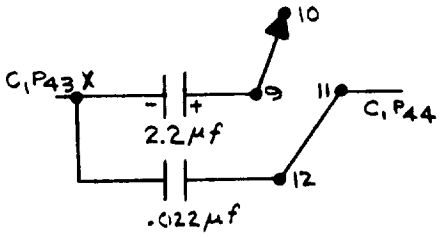
SEC C-3



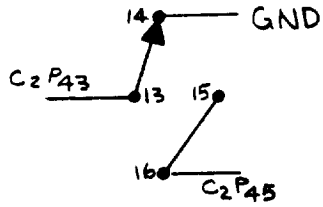
SEC C-4



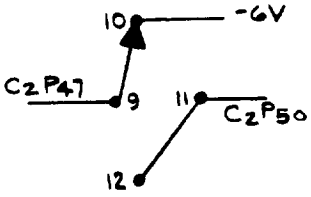
SEC D-3



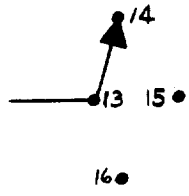
SEC D-4



SEC E-3

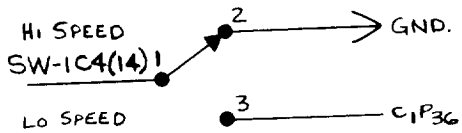


SEC E-4

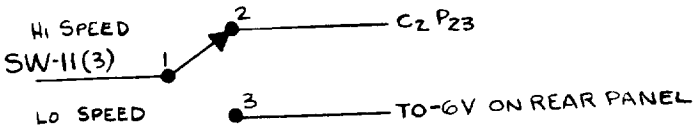


S-51

FIGURE 16-B



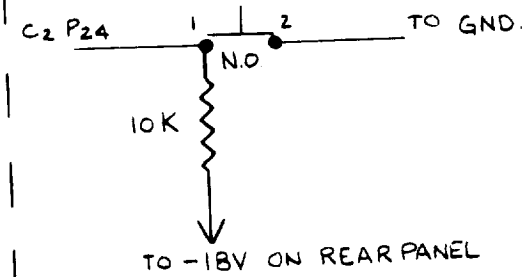
SECT A-1



SECT B-1

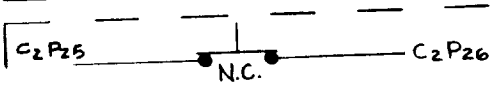
SWITCH-2

(2 POL. 2 POS./2 EXTRA WAFERS)



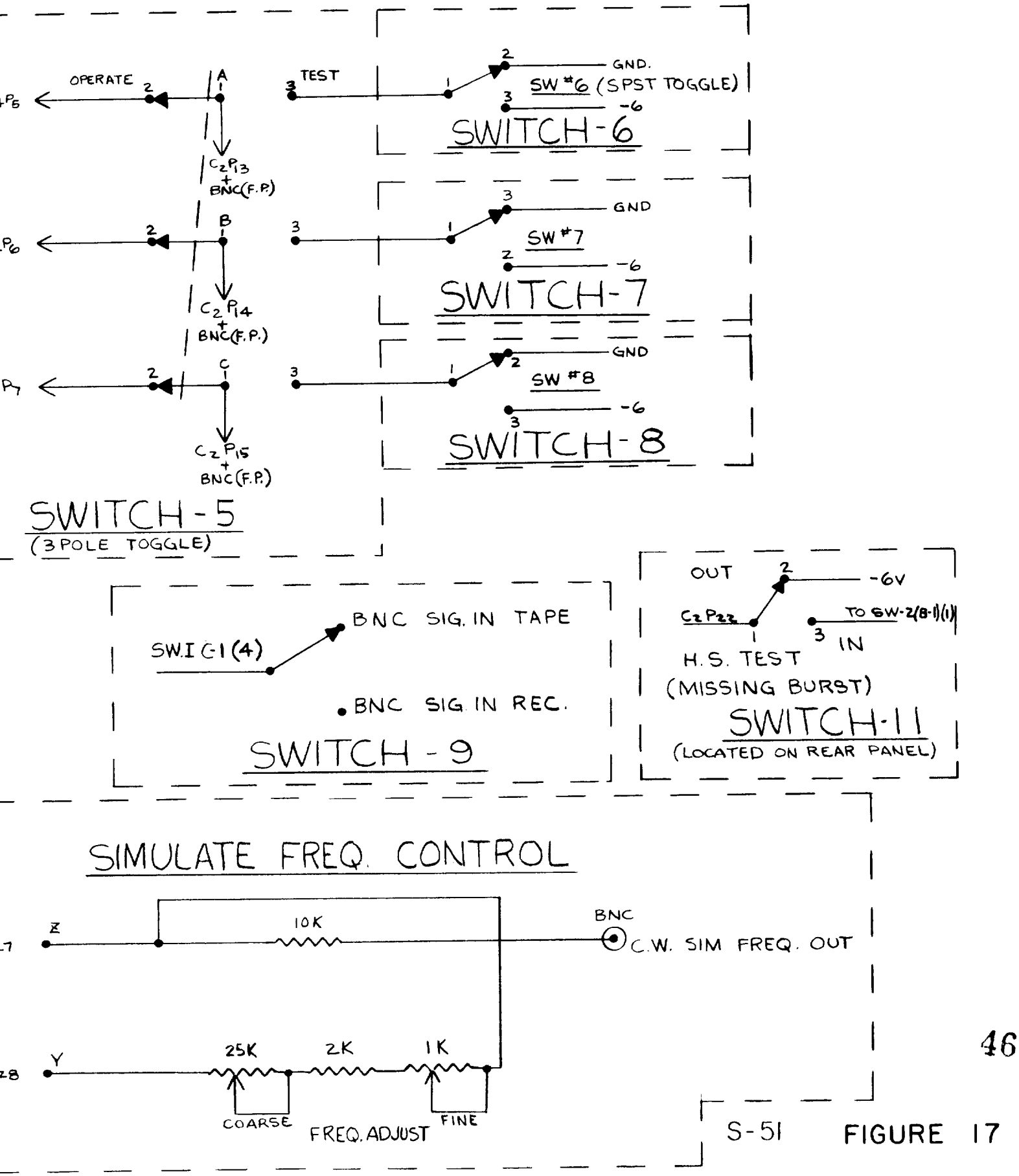
SWITCH-3

(PUSH BUTTON-NORMALLY OPEN)
MAN. RESET SEQ. COUNT



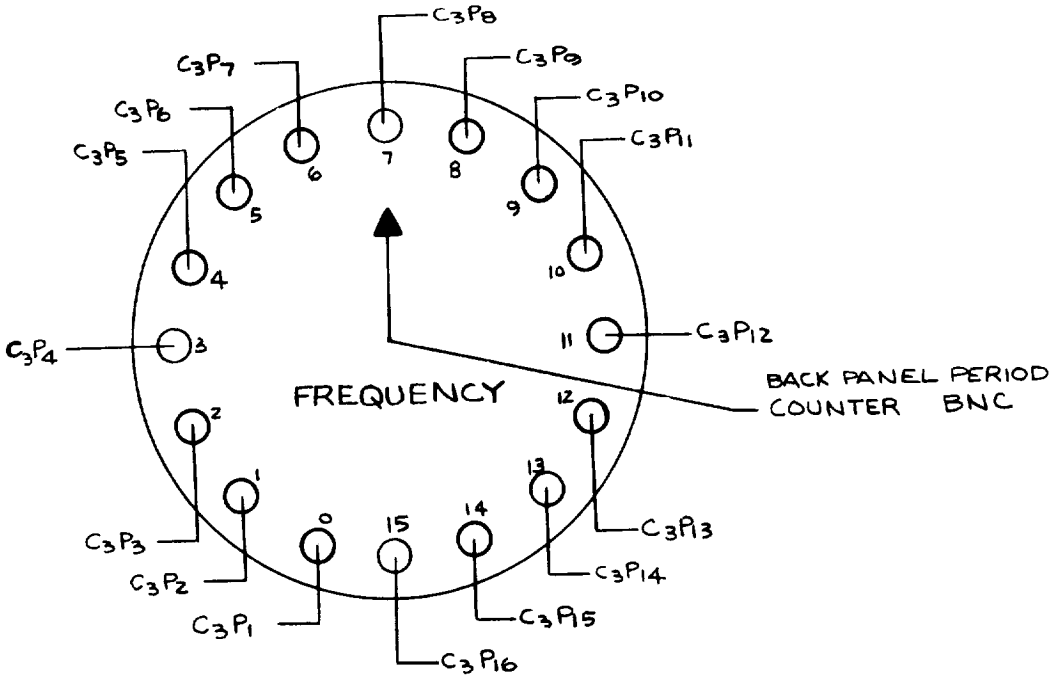
SWITCH-4

(PUSH BUTTON-NORMALLY CLOSED)
TEST MISSING SEQ COUNT

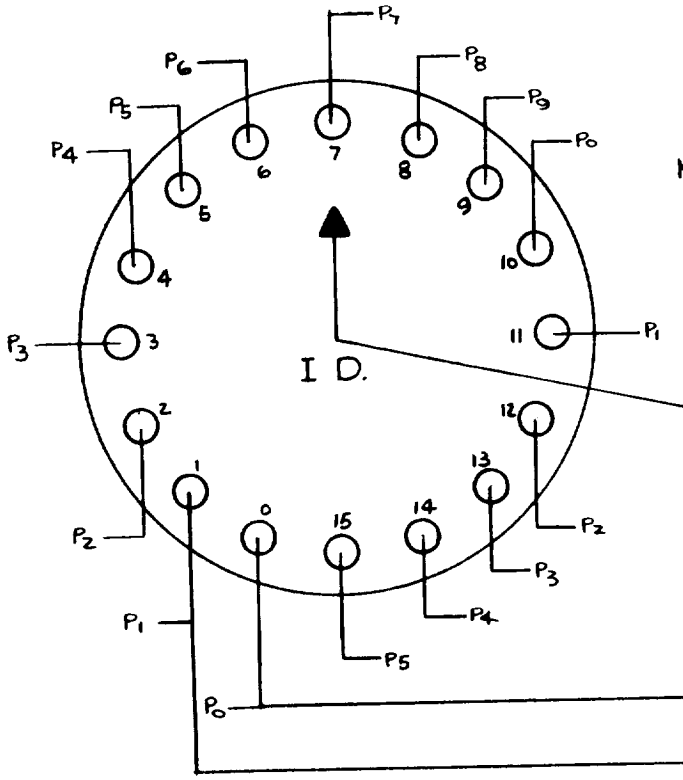


S-51 FIGURE 17

SWITCH #10
(CONTROL PANEL)

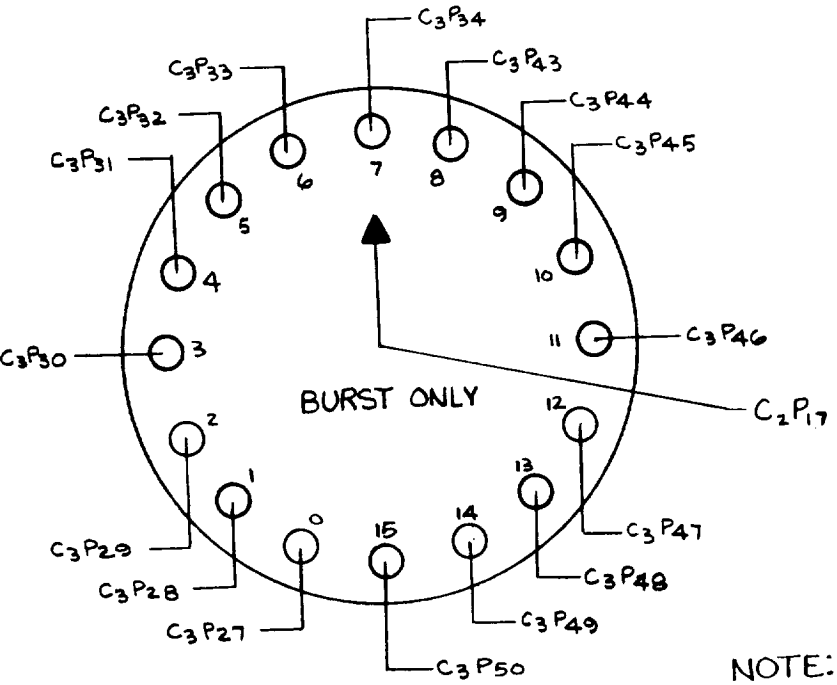


SECTION A



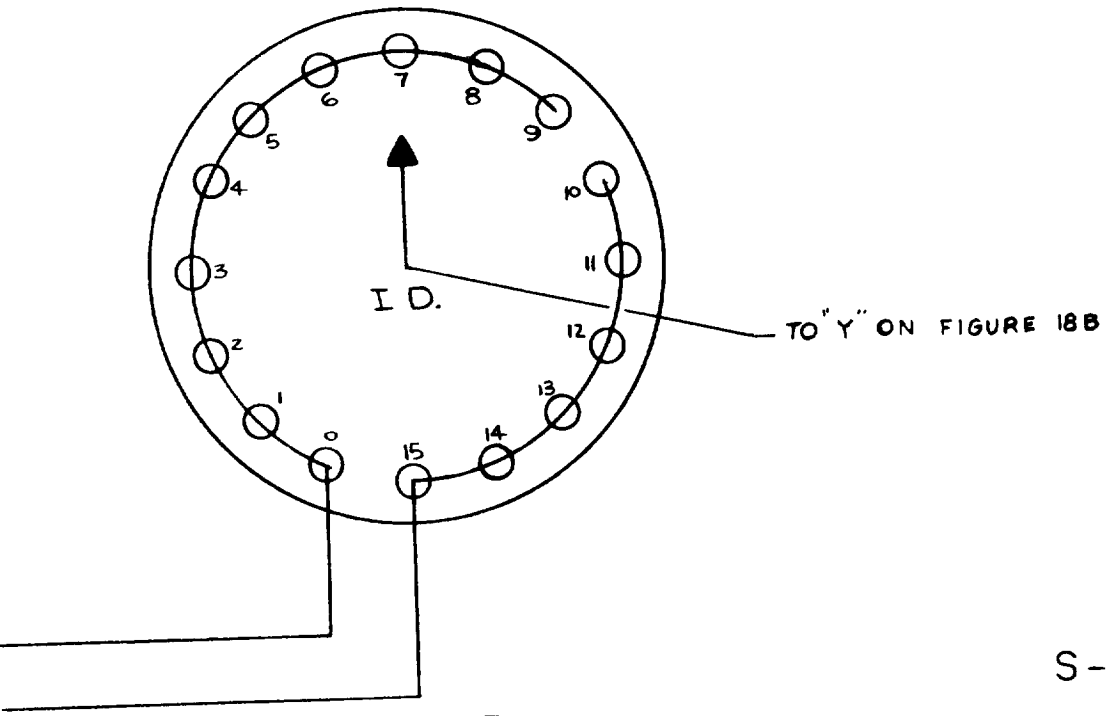
NOTE: SW. POS. 10-15 CONNECT WITH POS. 0-5 RESPECTIVELY

SECTION C



SECTION B

NOTE: POSITIONS 0-9 ON SECTION C TO VOLTAGE DIVIDER BOARD POINTS (P) 0-9 (SEE VOLTAGE DIVIDER BOARD CIRCUIT DIAGRAM FIGURE 18B.)

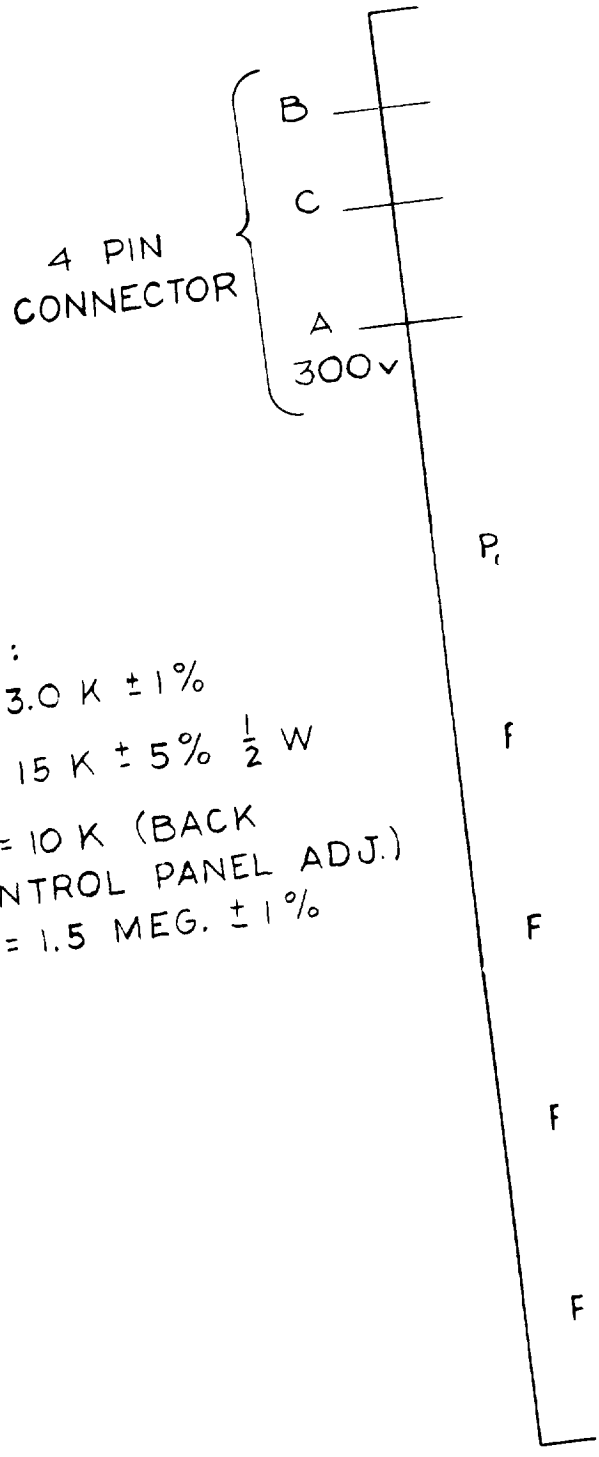


SECTION D

S-51 FIGURE 18A

CHANNEL IDENTIFICATIO

(MOUNTED IN CONTROL PA

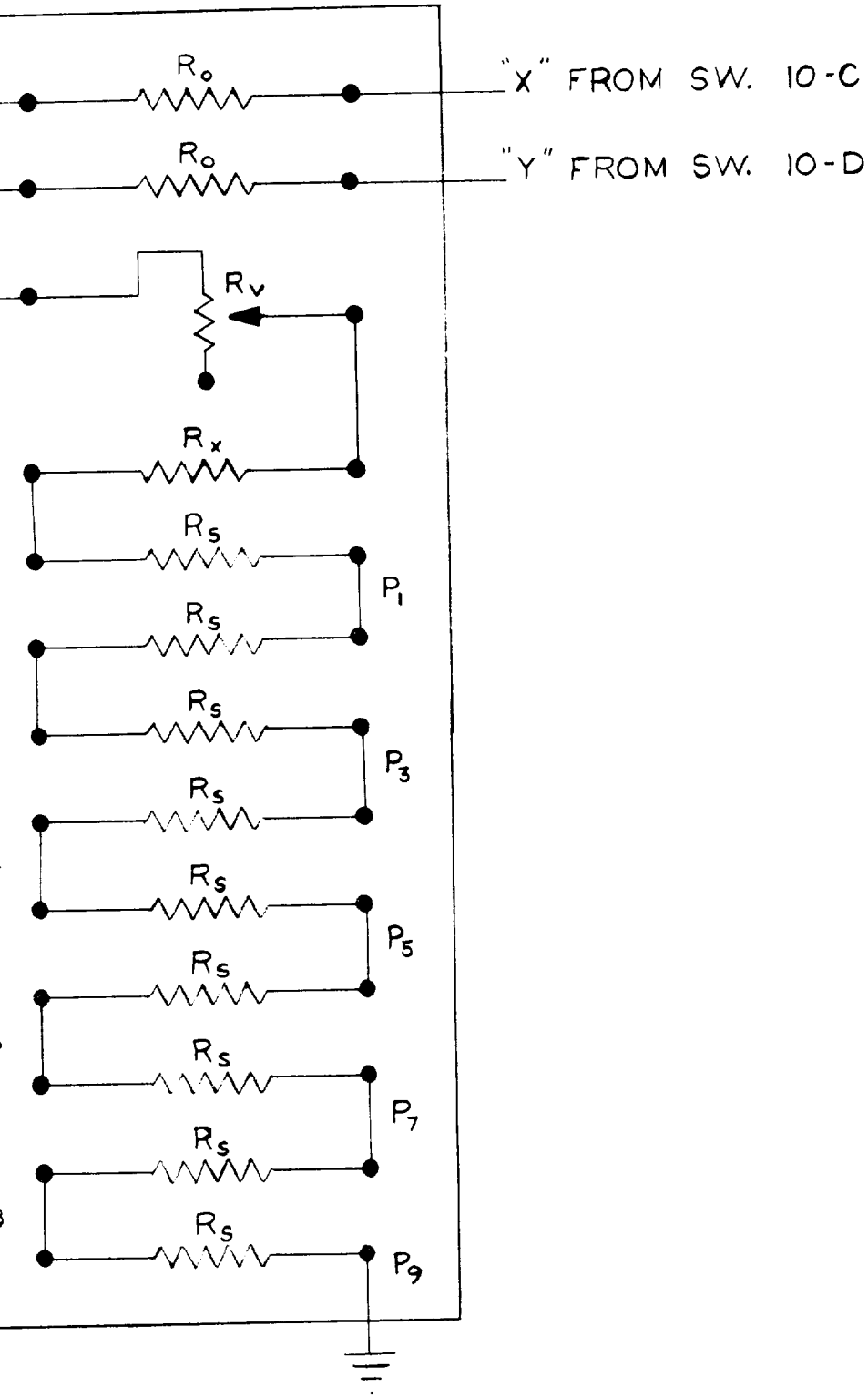


NOTES:

1. $R_S = 3.0\ K \pm 1\%$
2. $R_x = 15\ K \pm 5\%\ \frac{1}{2}\ W$
3. $R_V = 10\ K$ (BACK CONTROL PANEL ADJ.)
4. $R_o = 1.5$ MEG. $\pm 1\%$

VOLTAGE DIVIDER

EL BOX)



S-51 FIGURE 18B

				Connector #1	
	Reset Seq.Count		1	II-1
BNC	Out DIG " "		2	II-1
Connec-	Reset Dig. Flag		3	I-1
tors on	Flag out		4	II-1
Back	Sensi. Bit		5	III-
Control	Dec. No. in		6	I-1
Panel	Not used		7	I-1
	Dec. Count Stop		8	II-2
			9	
	SW-1	A-1(1)	10	II-
	SW-1	A-1(3)	11	II-
	SW-1	A-2(x)	12	II-
	SW-1	A-2(8)	13	II-
	SW-1	A-3(9)	14	II-
	SW-1	A-3(12)	15	II-
	SW-1	A-4(x)	16	II-
	SW-1	A-4(15)	17	II-
	SW-1	B-1(x)	18	II-
	SW-1	B-1(3)	19	II-
	SW-1	B-2(7)	20	II-
	SW-1	B-2(x)	21	II-
	SW-1	B-3(x)	22	II-
	SW-1	B-3(11)	23	II-
	SW-1	B-4(13)	24	II-1
			25	
	SW-1	B-4(14)	26	II-
			27	
			28	
	SW-1	C-1(3)	29	II-7
	SW-1	C-2(x)	30	II-2
	SW-1	C-2(7)	31	II-2
	SW-1	C-3(x)	32	II-1
	SW-1	C-3(11)	33	II-1
	SW-1	C-4(13)	34	II-1
			35	
	SW-2	A-1(3)	36	II-
	SW-1	B-1(2)	37	II-
			38	
	SW-1	B-1(1)	39	II-1
	SW-1	B-2(6)	40	II-
			41	
	SW-1	B-2(5)	42	I-1
	SW-1	B-3(x)	43	I-2
	SW-1	B-3(11)	44	I-2
BNC START DEC.COUNT			45	III-
			46	
	C4 P10		47	II-2
	C3 P26		48	III-
SAME AS *50 (ON *1 UNIT)			49	
	OUT ANALOG SEQ. COUNT		50	III-19

Connector #2

C3 P27	1	I-23-17	"0" Burst.Envel. (po
C3 P28	2	I-23-11	"1" " "
C3 P29	3	I-24-20	"2" " "
C3 P30	4	I-24-19	"3" " "
C3 P43	5	I-24- 9	"8" " "
C3 P44	6	I-25-11	"9" " "
C3 P45	7	I-25- 9	"10" " "
C3 P46	8	I-26-20	"11" " "
C3 P49	9	I-26-17	"14" " "
C3 P50	10	I-26-11	"15" " "
	11		
C3 P40	12	I-23-20 Decom. Envel. Out.(neg.	
SW5 A-1	13	I-15-20 2^0 (from Comb.Fil)(neg.	
SW5 B-1	14	I-15-31 2^1 " " " "	
SW5 C-1	15	I-15-22 2^2 " " " "	
C3 P36	16	III- 2- 6 Decom. Bd. #2 input	
	17	I-28-18 Burst Envel. Switched	
To SW#10 B	18	I-28- 6 to Strip Chart	
to BNC	19		
	20		
	21		
SW 11(1)	22	II- 5-10	
SW 2 B-1(3)	23	II- 8-29	
SW 3 (1)	24	II-19-22	
SW 4 (1)	25	II-10-27	
SW 4 (2)	26	II-18-31,22; II-19-18	
S.F.C. s	27	II- 7- 8 Sim. Freq. Cont. Pots &	
S.F.C. y	28	II- 7-10 " " "	
	29		
-18v to volt on Rear Panel	30	-18 Pin-2 on all S-Blocs	
	31		
- 6v to volt on Rear Panel	32	- 6 Pin-3 on all S-Blocs	
	33		
+12v to volt on Rear Panel	34	+12 Pin-4 on all S-Blocs	
	35		
GND to on Rear Panel	36	GND Pin-5 on all S-Blocs	
	37		
SW 1 E-2(5)	38	II-18-12	
SW 1 E-2(8)	39	II- 3-19; II- 6-19	
SW 1 E-1(4)	40	III- 3- 7	
SW 1 E-1(1)	41	III- 3-13	
	42		
SW 1 D-4(13)	43	III- 9-20	
	44		
SW 1 D-4(16)	45	II-16- 6	
Input Sig. Sensor Out	46	II-16-24	
SW 1 E-3(9)	47	III- 2-15 orange	
	48		
On 1st 8-5} only.SW1 E-3(10)	49	-6v green	
SW 1 E-3(11)	50	III-11-31	

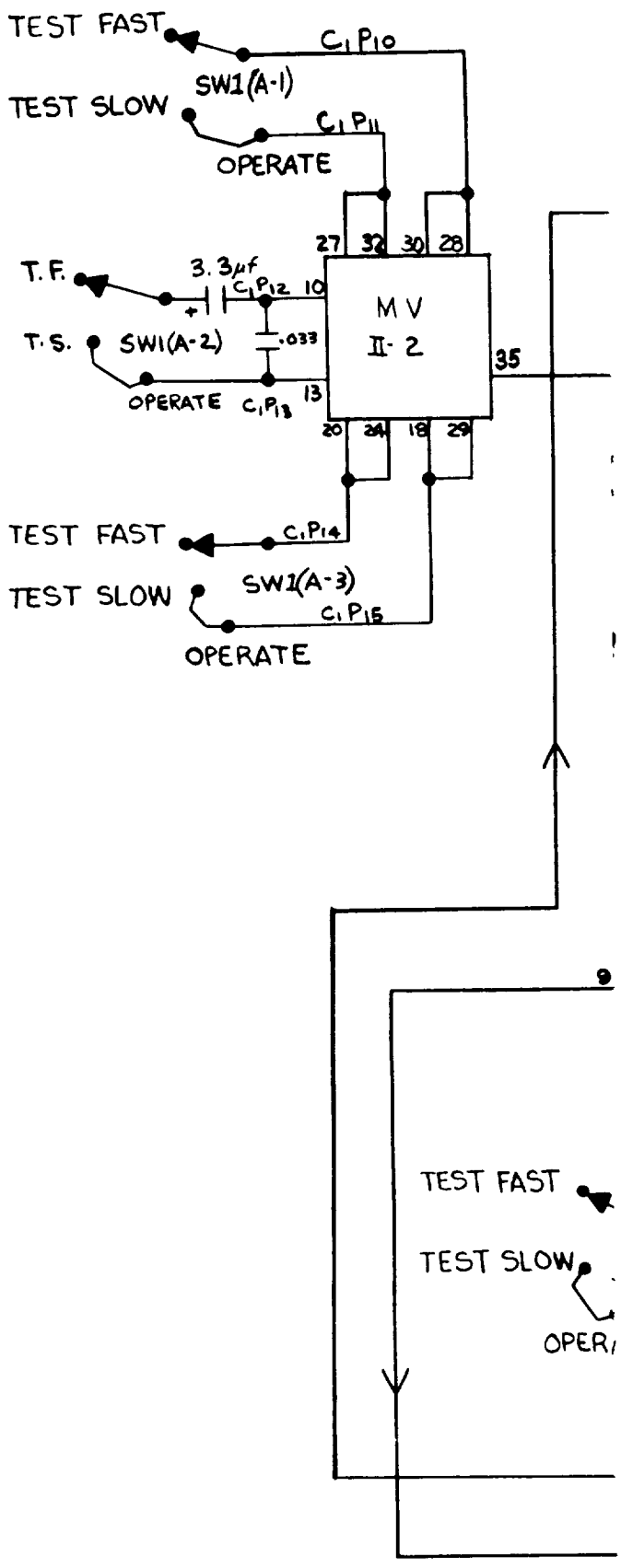
S-BLOC CONNECTORS

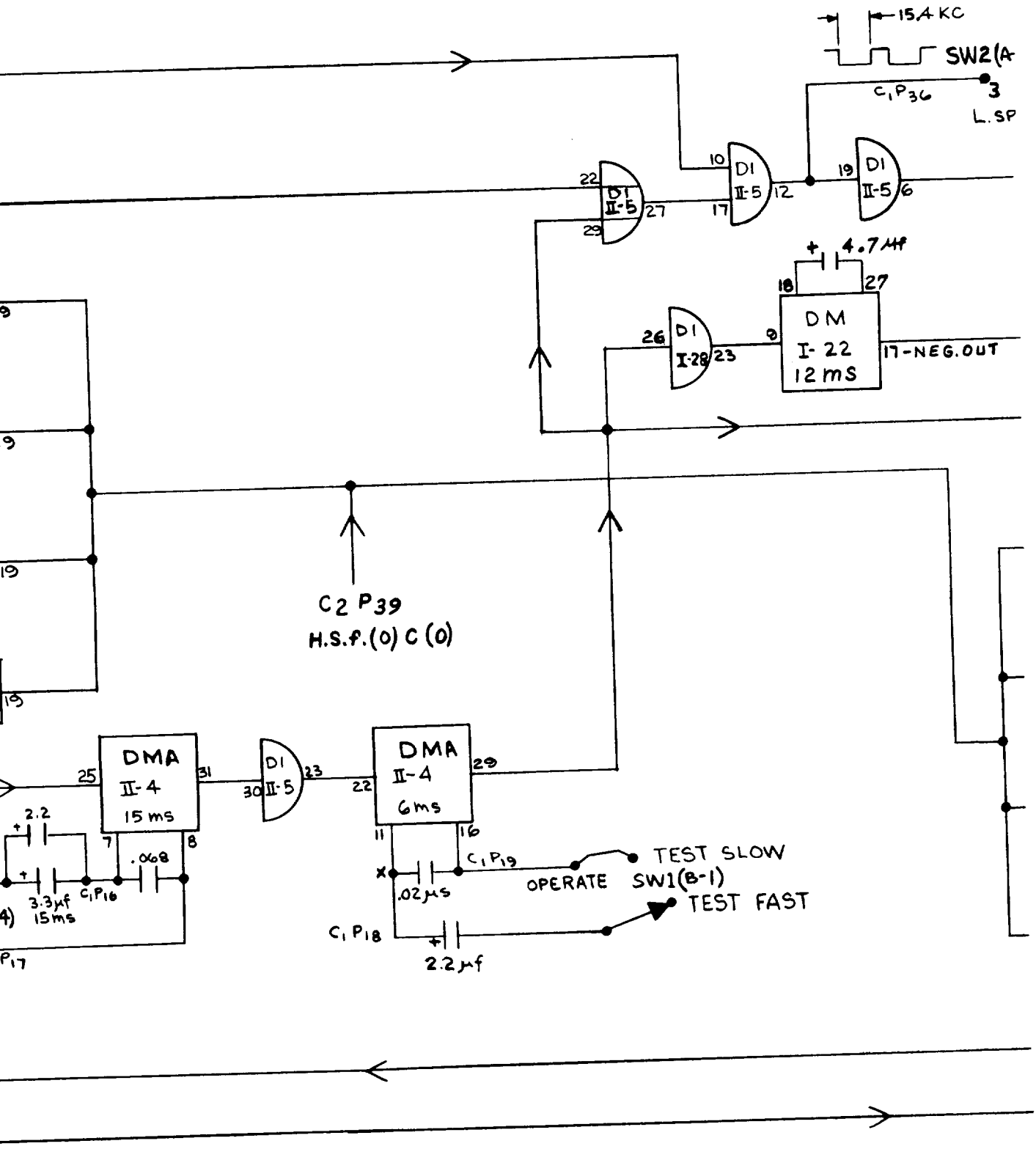
SW#10(A) BNC's on Back Control Panel

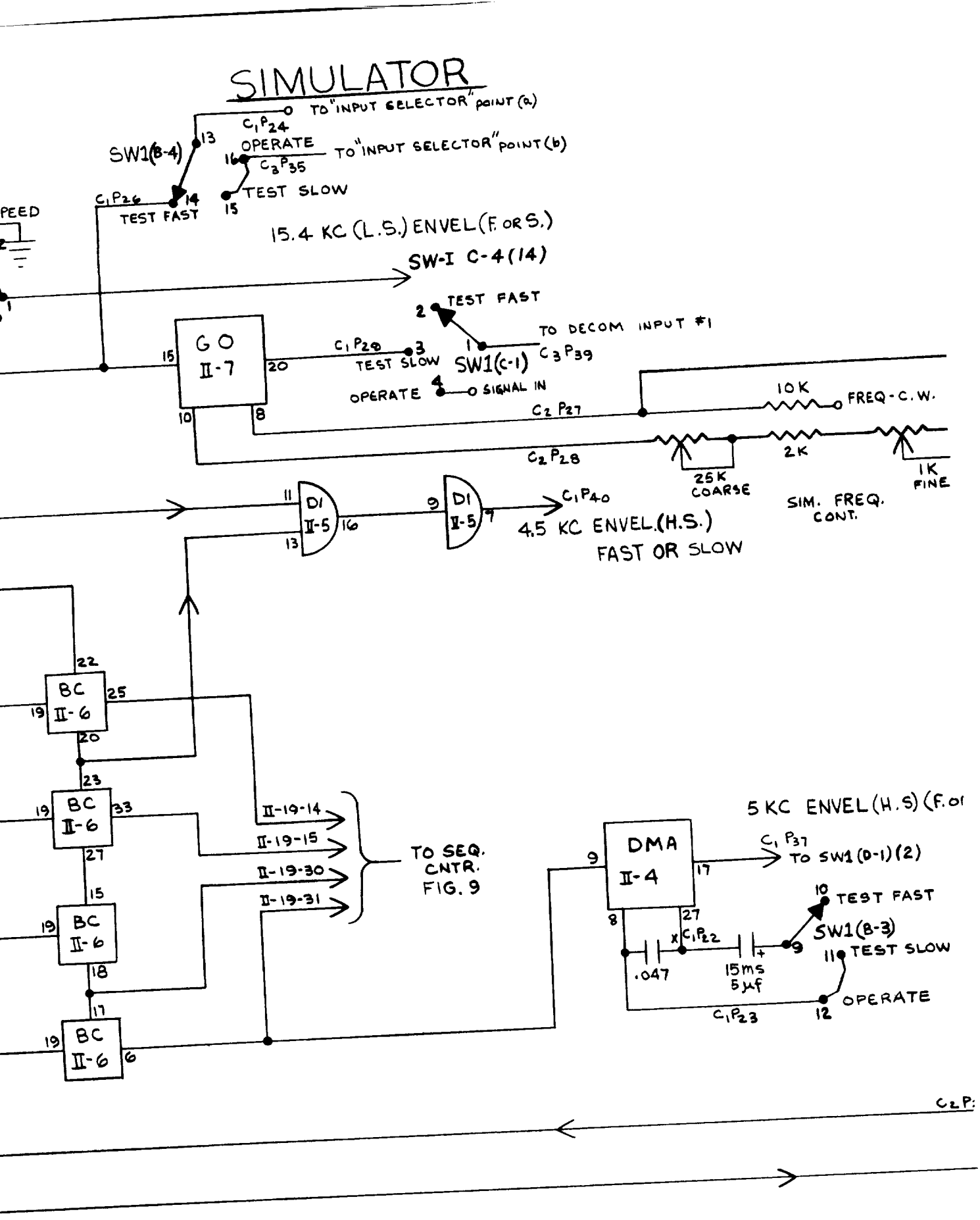
	Connector #3 - Decom.	
	1	BBF 0
	2	" 1
	3	" 2
	4	" 3
	5	" 4
	6	" 5
	7	" 6
	8	" 7
	9	" 8
	10	" 9
	11	" 10
	12	" 11
	13	" 12
	14	" 13
	15	" 14
	16	" 15
	17	
	18	
	19	
	20	
Power SW	21	AC-1
Power SW	22	AC-1
	23	
Power SW	24	AC-2
Power SW	25	AC-2
C1 P48	26	Board #2 Pin 5
SW#10 & C2 P1	27	Burst Only 0
SW#10 & C2 P2	28	" " 1
SW#10 & C2 P3	29	" " 2
SW#10 & C2 P4	30	" " 3
SW#10	31	" " 4
SW#10	32	" " 5
SW#10	33	" " 6
SW#10	34	" " 7
Input to Buffer Amp.	35	Bd. #1 Out
C2 P16	36	Bd. #2 In
	37	
C4 P10	38	AGC Out (to C.F.)
SW-1 C-1(1)	39	Video In
C2 P12	40	Envelop Out (Neg.going)
GND	41	GND
GND	42	GND
SW#10 & C2 P5	43	Burst Only 8
SW#10 & C2 P6	44	" " 9
SW#10 & C2 P7	45	" " 10
SW#10 & C2 P8	46	" " 11
SW#10	47	" " 12
SW#10	48	" " 13
SW#10 & C2 P9	49	" " 14
SW#10 & C2 P10	50	" " 15

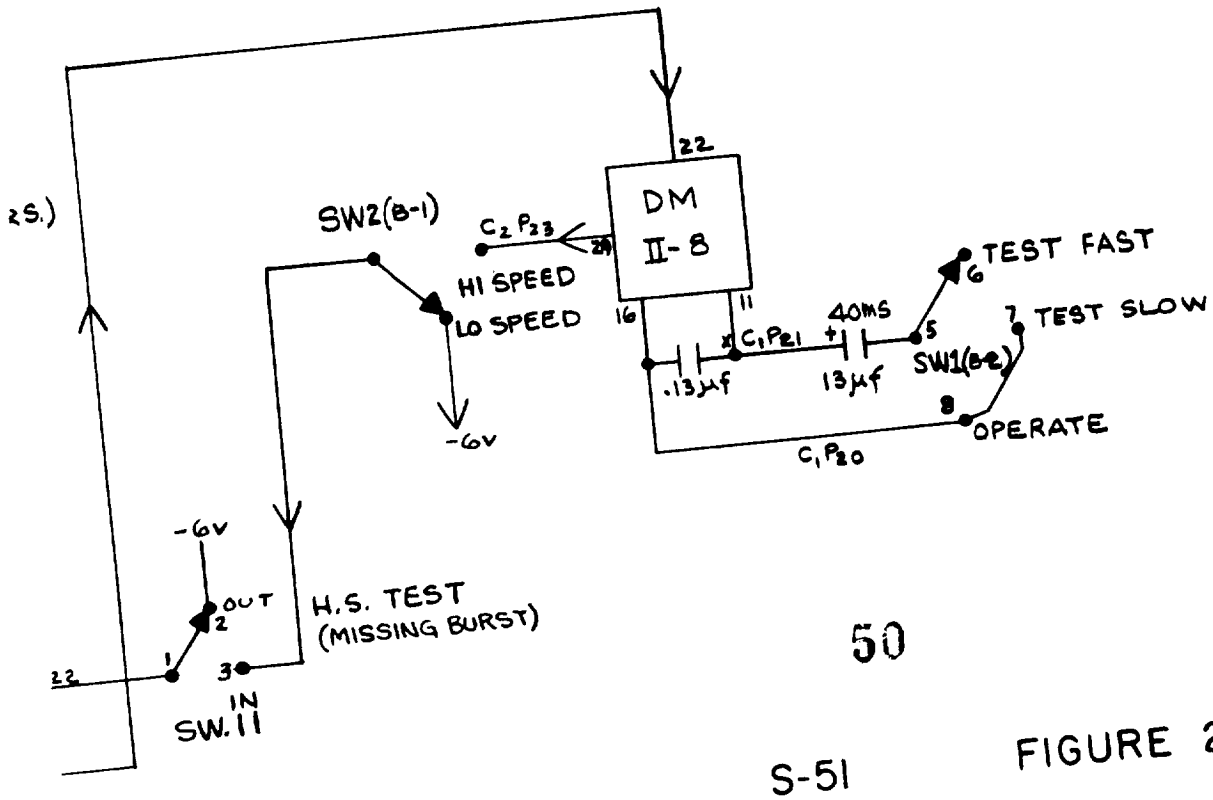
Connector #4 - Comb Filter		
	1	Ac out to Fan
	2	Ac out to Fan
SW1 D-1(4)	3	Comb Fil. 5KC Envel. neg. going
SW1 D-2(8)	4	" " 4.5KC " " "
SW5 A-2	5	2^8 neg. going
SW5 B-2	6	2^4 neg. going
SW5 C-2	7	2^2 neg. going
PWR SW (1)	8	ac in
PWR SW (2)	9	ac in
C3 P38 & C1 P47	10	Input (agc from decom)
SW1 C-4(16)	11	Comb Fil 15.4 KC Envel.
	12	
GND	13	GND
GND	14	GND
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	

FIGURE 19


TEST FAST
C1 P10
SW1(A-1)
TEST SLOW
C1 P11
OPERATE
27
32
30
28
T.F.
3.3μf
C1 P12
10
MV
II-2
T.S.
SW1(A-2)
.033
35
OPERATE
C1 P13
13
20
24
18
29
TEST FAST
C1 P14
TEST SLOW
SW1(A-3)
C1 P15
OPERATE
9
TEST FAST
TEST SLOW
OPER


15.4 KC
SW2(A
C1P36
3
L.SP
D1 II-5
4.7 μf
DM I-22 12 ms
17-NEG.OUT
D1 I-28
C2 P39
H.S.F.(0) C (0)
DMA II-4 15 ms
DMA II-4 6 ms
2.2
.068
3.3μf 15ms
C1P16
C1P17
.02μs
C1P19
C1P18
2.2μf
TEST SLOW
OPERATE
SW1(B-1)
TEST FAST


SIMULATOR
TO "INPUT SELECTOR" POINT (a)
C1P24
SW1(B-4)
OPERATE
TO "INPUT SELECTOR" POINT (b)
C3P35
C1P26
TEST FAST
TEST SLOW
15.4 KC (L.S.) ENVEL (F. OR S.)
SW-I C-4 (14)
TEST FAST
TO DECOM INPUT #1
GO II-7
C1P29
TEST SLOW
SW1(C-1)
C3P39
OPERATE
SIGNAL IN
C2P27
10K
FREQ-C.W.
C2P28
25K COARSE
2K
1K FINE
SIM. FREQ. CONT.
DI II-5
DI II-5
C1P40
4.5 KC ENVEL. (H.S.)
FAST OR SLOW
BC II-6
BC II-6
BC II-6
BC II-6
II-19-14
II-19-15
II-19-30
II-19-31
TO SEQ. CNTR. FIG. 9
5 KC ENVEL (H.S) (F. or
DMA II-4
C1P37
TO SW1 (D-1) (2)
TEST FAST
SW1(B-3)
TEST SLOW
OPERATE
C1P22
.047
15ms 5μf
C1P23
C2P:



S-51

FIGURE 20

S-51 FIGURE 21

	0	1	2	3 H	4 I	5 G	6 H	7	8 S	9 P	10 E	11 E	12 D	13	14	15	0
0	PRINT X'S RESET REG. AFTER X'S	LOAD C_1	LOAD C_2	LOAD C_3													
1	SET FLAG CNTR TO ZERO-SET DEC. COUNT TO ZERO AFTER X'S	DELAY, READ C_{1-4} LOAD C_4	PRINT IST C_{1-4} LOAD C_5	LOAD C_6													
2	SET DEC. COUNT TO ZERO AFTER C_{1-4}	READ C_{5-6} TO DEC. COUNT															
3																	
4	PRINT C_{5-6}																
5																	
6																	
7																	
8	RESET REG TO ZERO	LOAD C_1	LOAD C_2	LOAD C_3													
9	SET DEC. COUNT TO ZERO AFTER IST C_{5-6}	DELAY READ C_{1-4} LOAD C_4	PRINT C_{1-4} LOAD C_5	LOAD C_6													
10	SET DEC. COUNT TO ZERO AFTER 2ND C_{1-4}	READ C_{5-6} TO DEC. COUNT															
11																	
12	PRINT C_{5-6}																
13																	
14	RESET REG TO ZERO AFTER 2ND C_{5-6}		LOAD X_1	LOAD X_2													
15		RESET DEC COUNT LOAD X_3	LOAD X_4	READ X'S LOAD X_5													
16																	
					L	O	W		S	P	E	E	D				
0				SET REG TO ZERO					RESET DEC COUNT AND FLAG LOAD C_1	LOAD C_2	LOAD C_3	READ C_{1-4} LOAD C4		PRINT C_{1-4}	LOAD C_5	LOAD C_6	
1									SET ZERO AFTER C_{1-4}	READ OUT C_{5-6}	PRINT C_{5-6}						

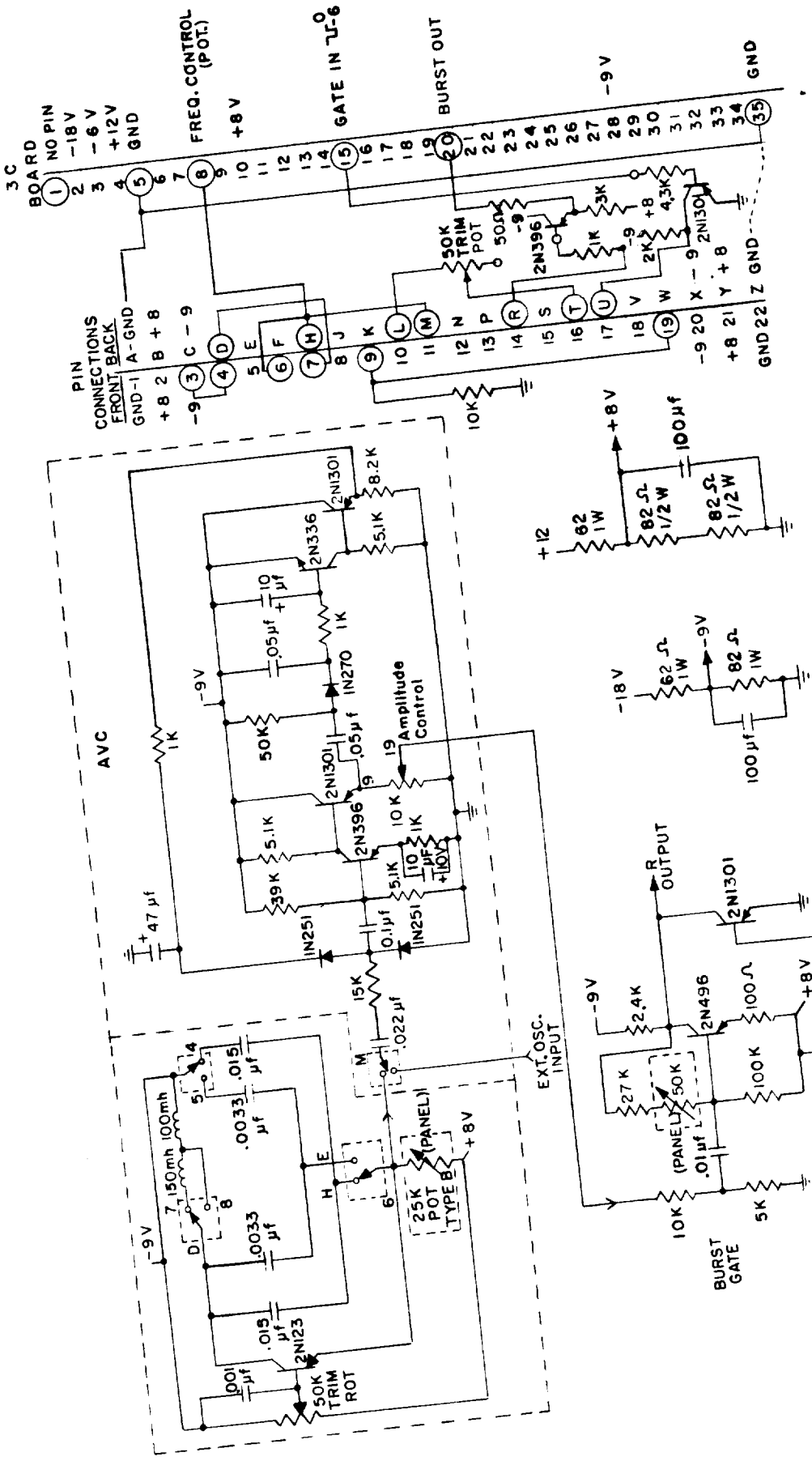
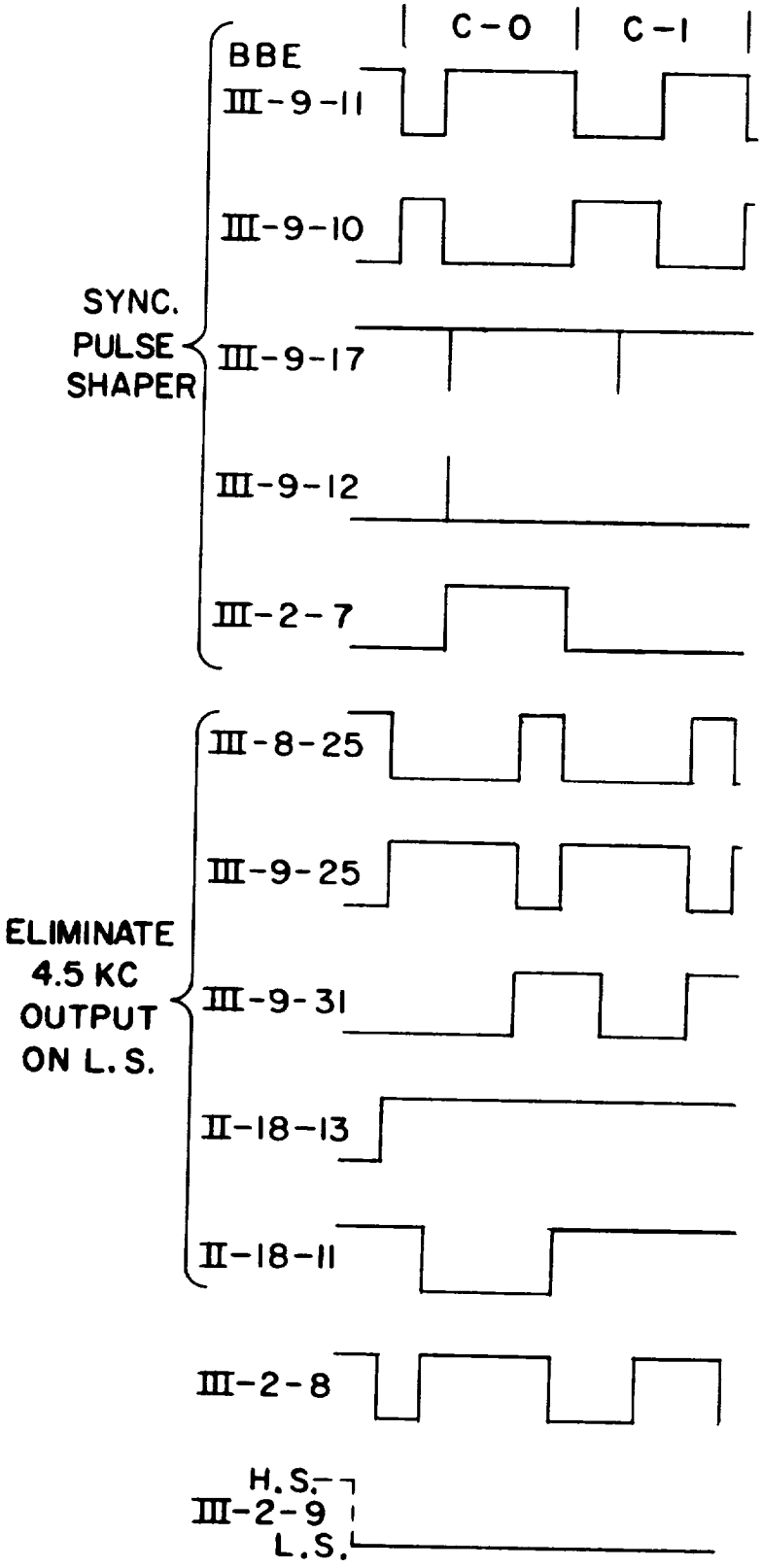
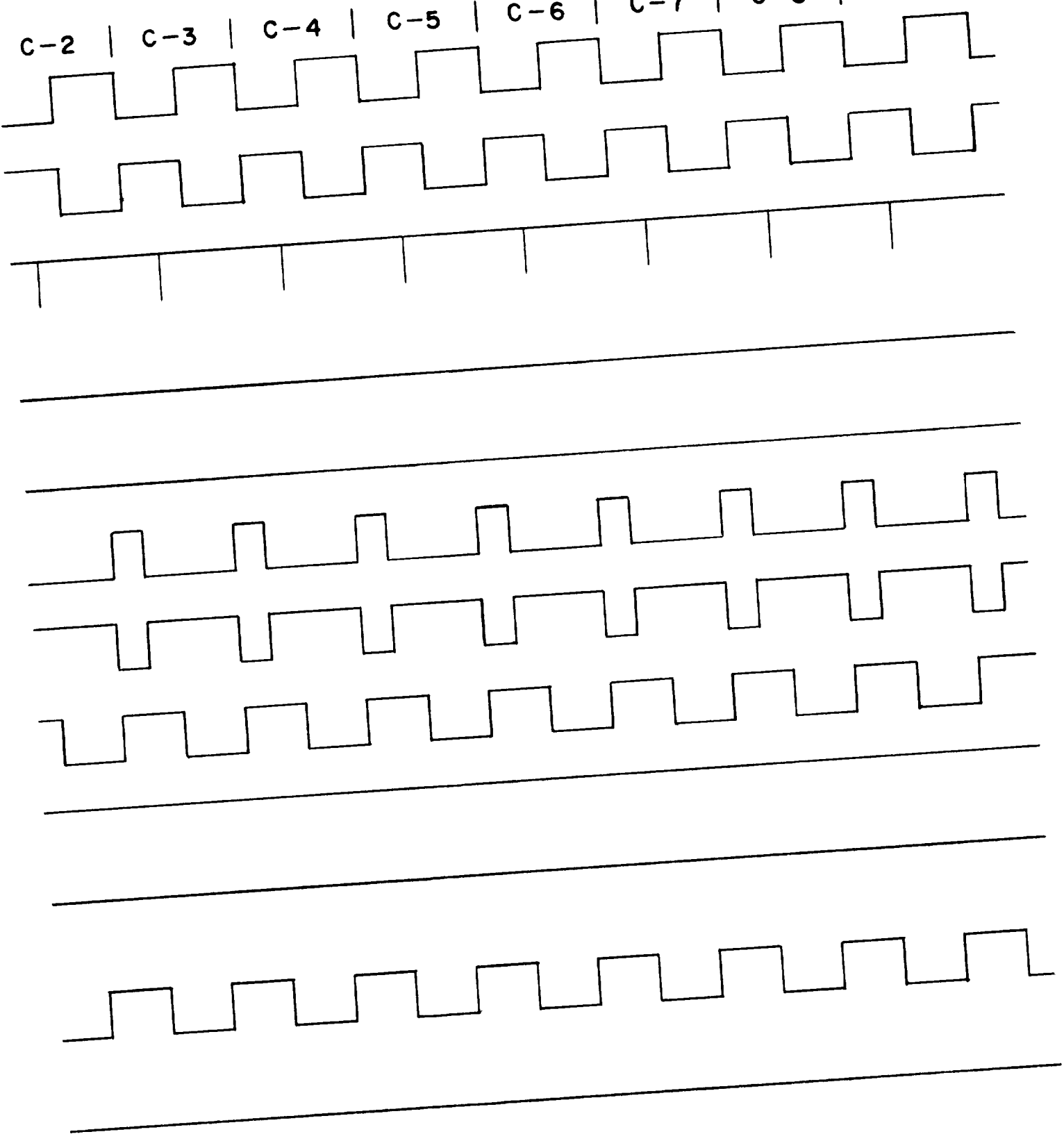


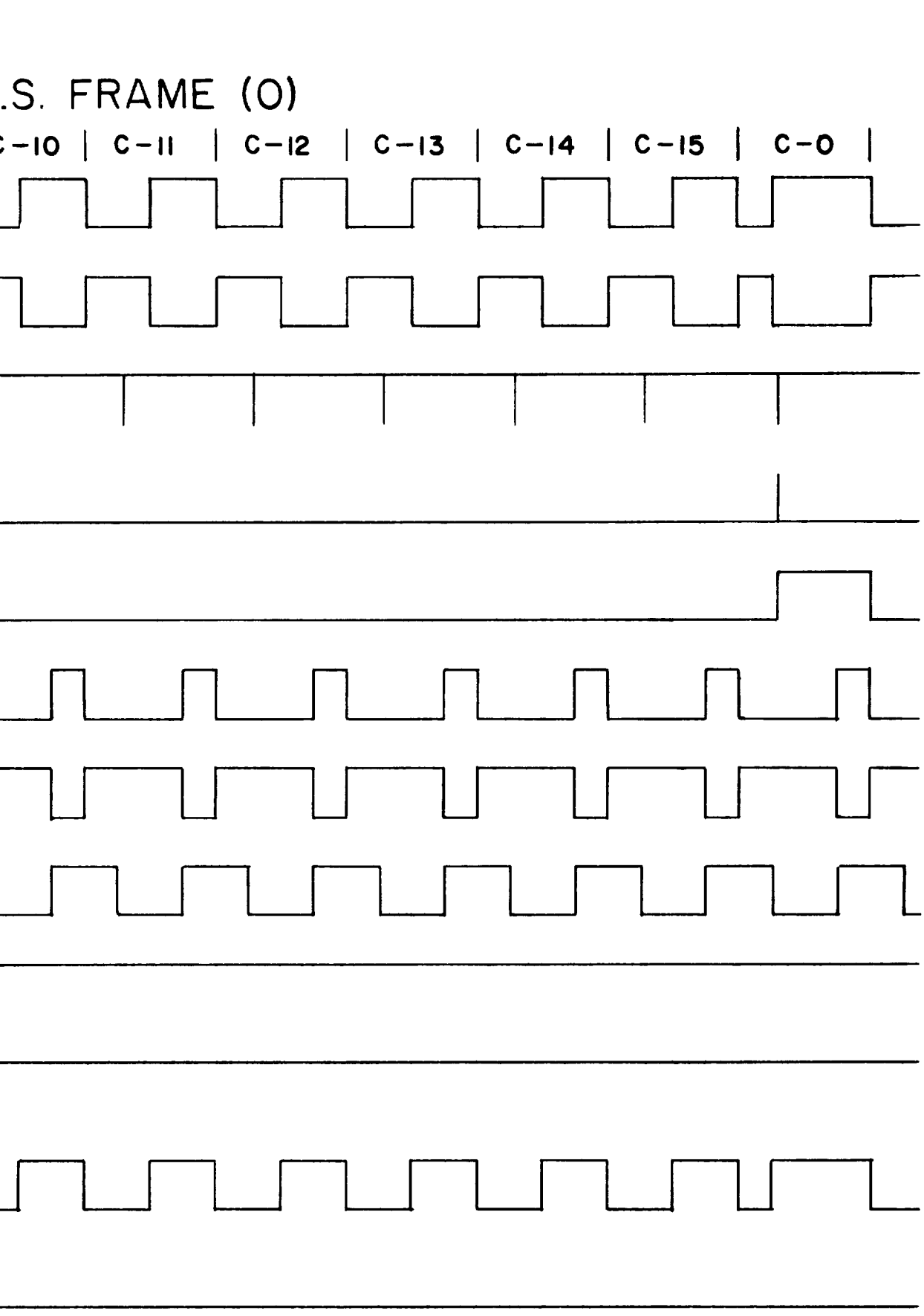
FIG. 22

S-51 SIMULATOR OSC. BOARD


C-0
C-1
BBE
III-9-11
III-9-10
SYNC. PULSE SHAPER
III-9-17
III-9-12
III-2-7
III-8-25
III-9-25
ELIMINATE 4.5 KC OUTPUT ON L.S.
III-9-31
II-18-13
II-18-11
III-2-8
H.S.
III-2-9
L.S.

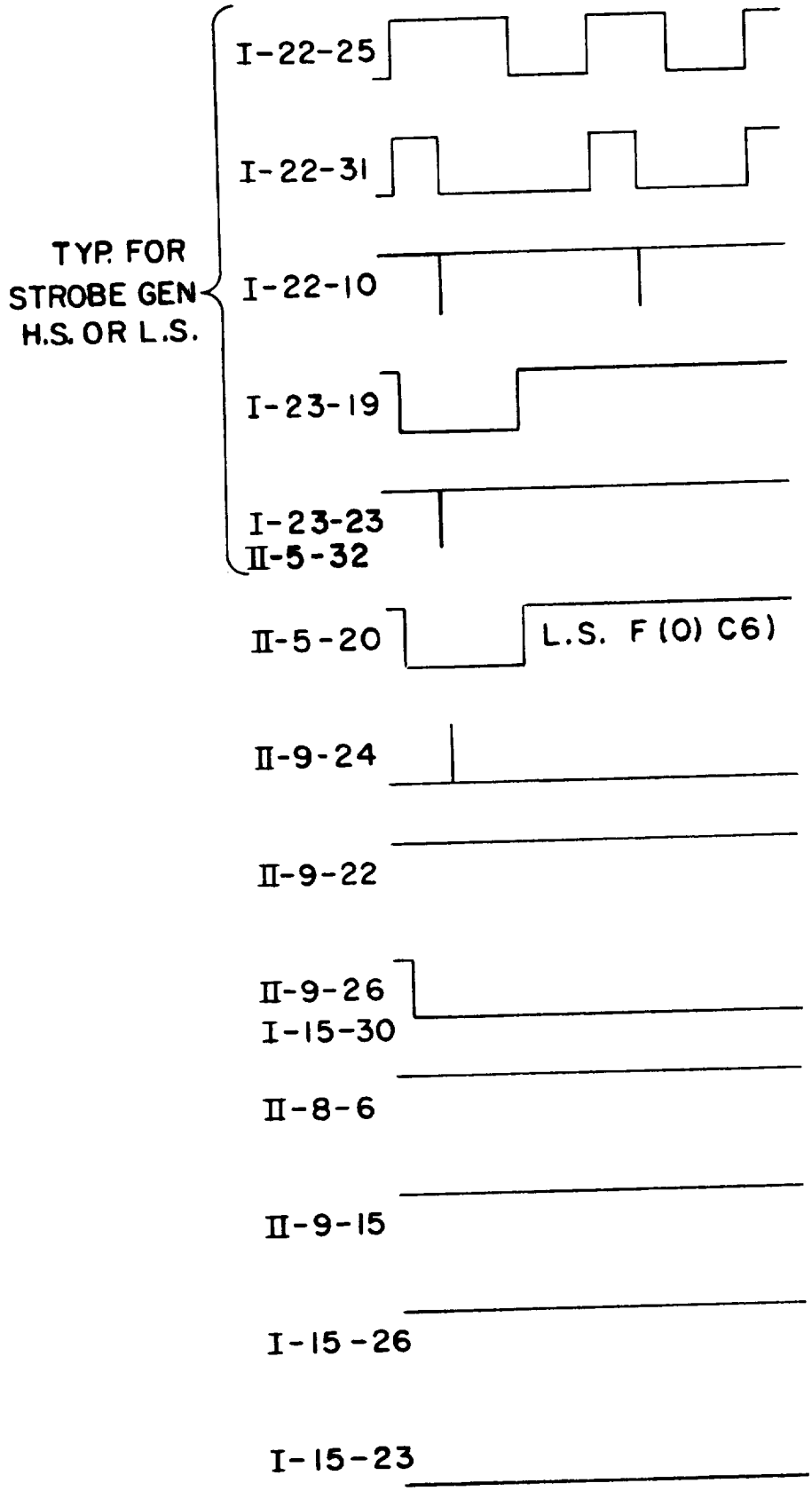
INPUT SELECTOR TIMING ON L



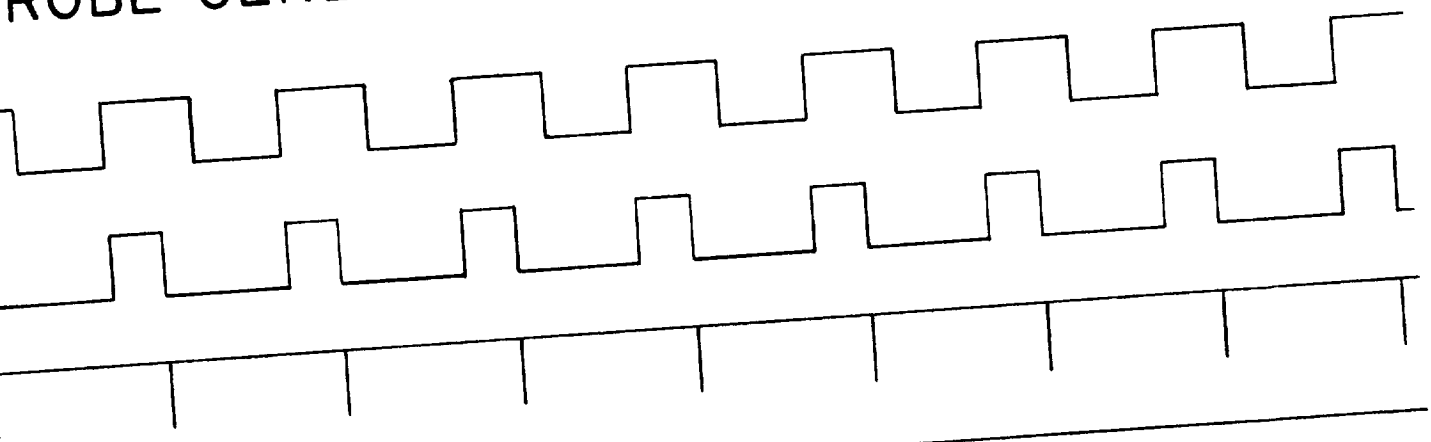


S-51 FIGURE 23

S


TYP. FOR
STROBE GEN
H.S. OR L.S.
I-22-25
I-22-31
I-22-10
I-23-19
I-23-23
II-5-32
II-5-20
L.S. F (0) C6)
II-9-24
II-9-22
II-9-26
I-15-30
II-8-6
II-9-15
I-15-26
I-15-23

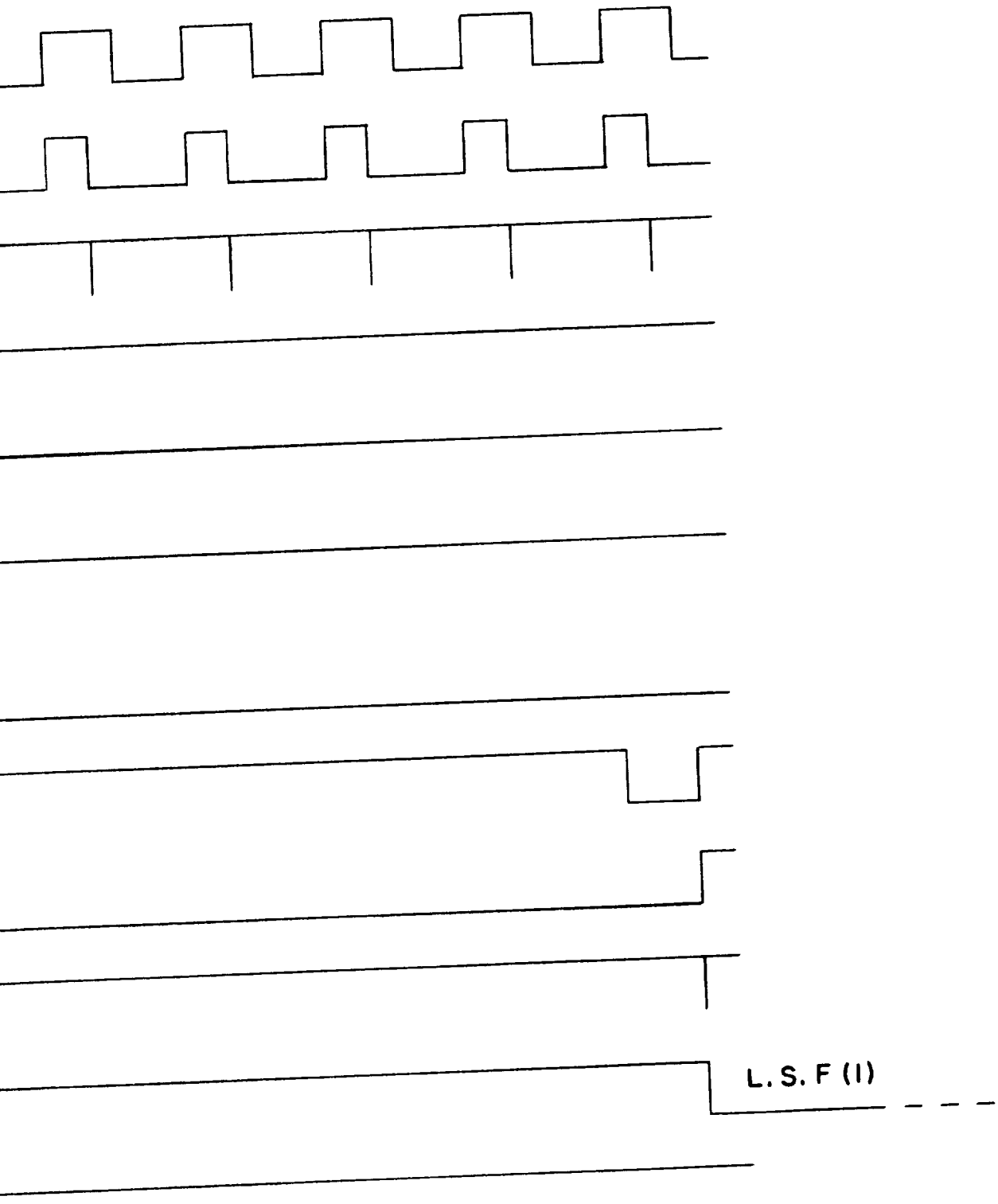
ROBE GENERATOR, L.S. FRAME SORTER, AND



L.S. F (0)

TYPICAL OUTPUT O

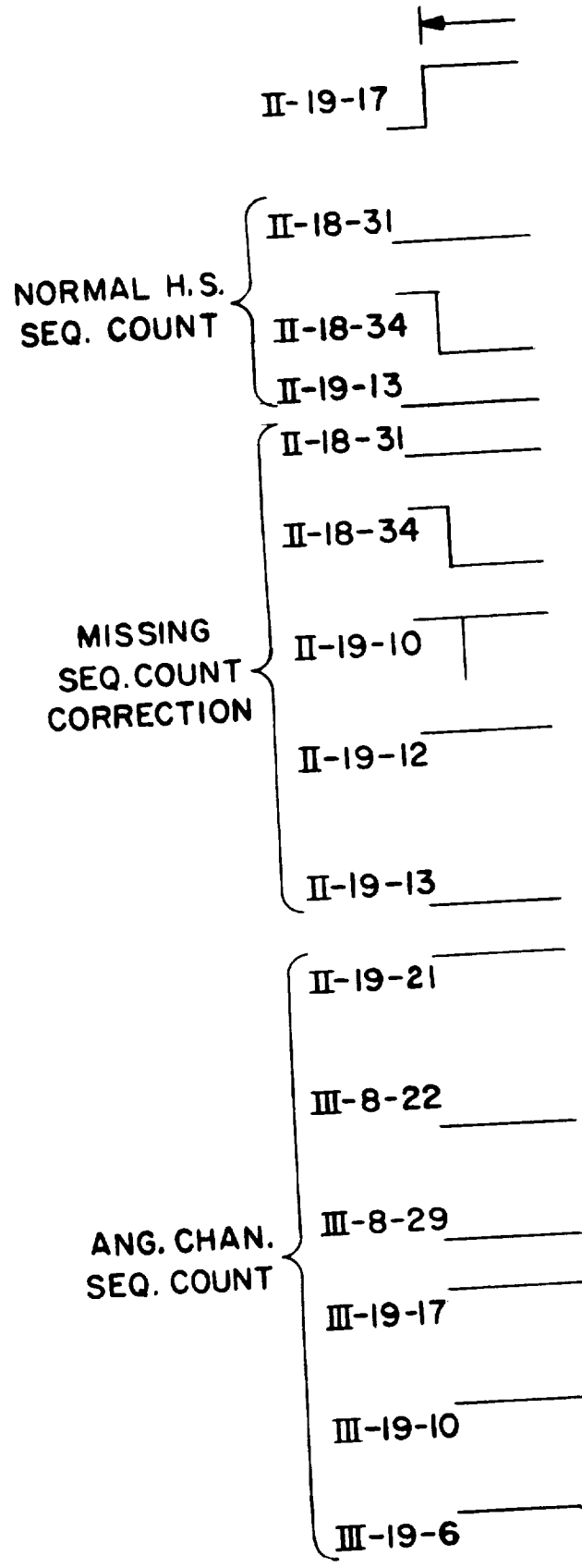
S. PROGRAMMER TIMING



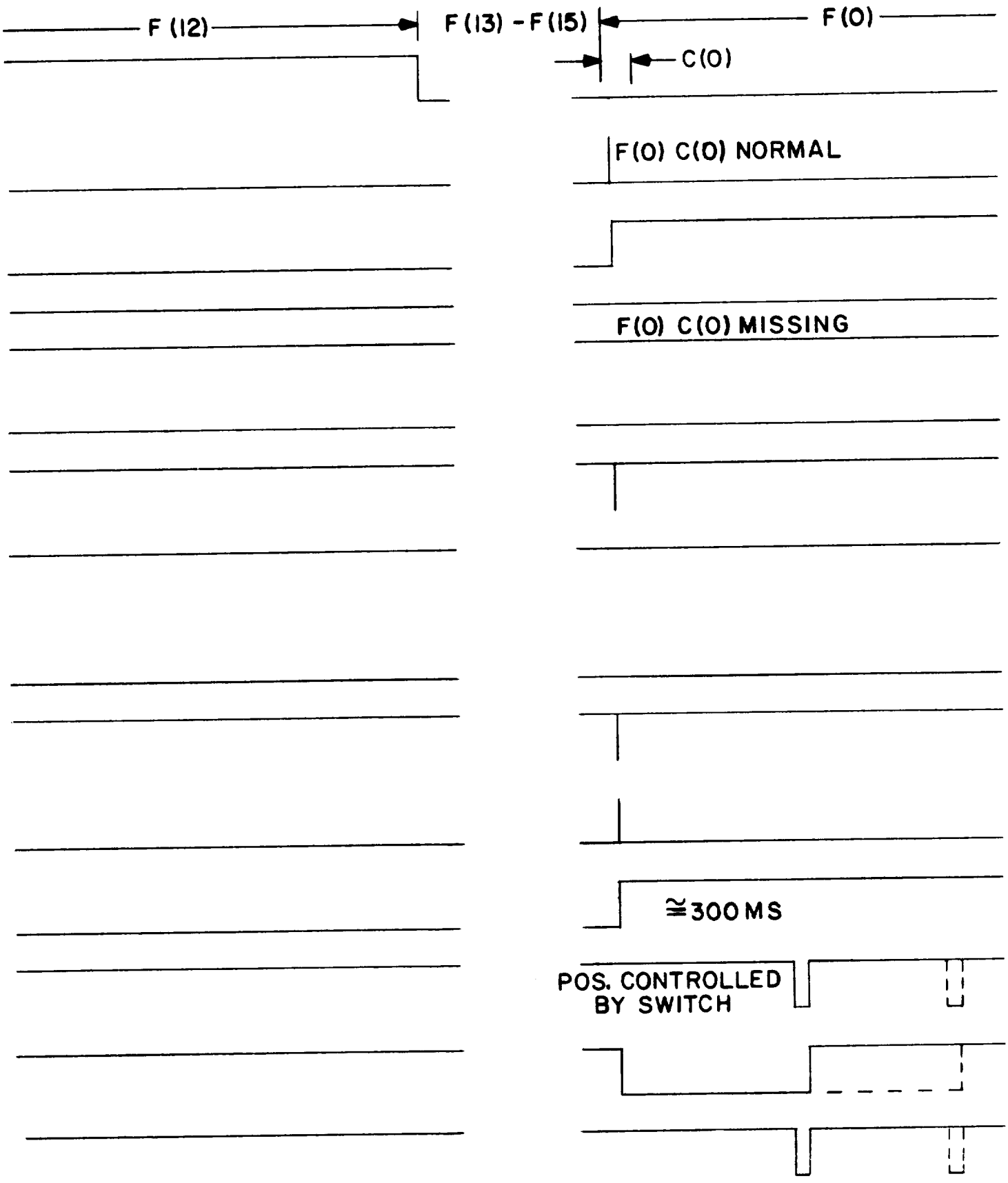
S-51

FIGURE 24

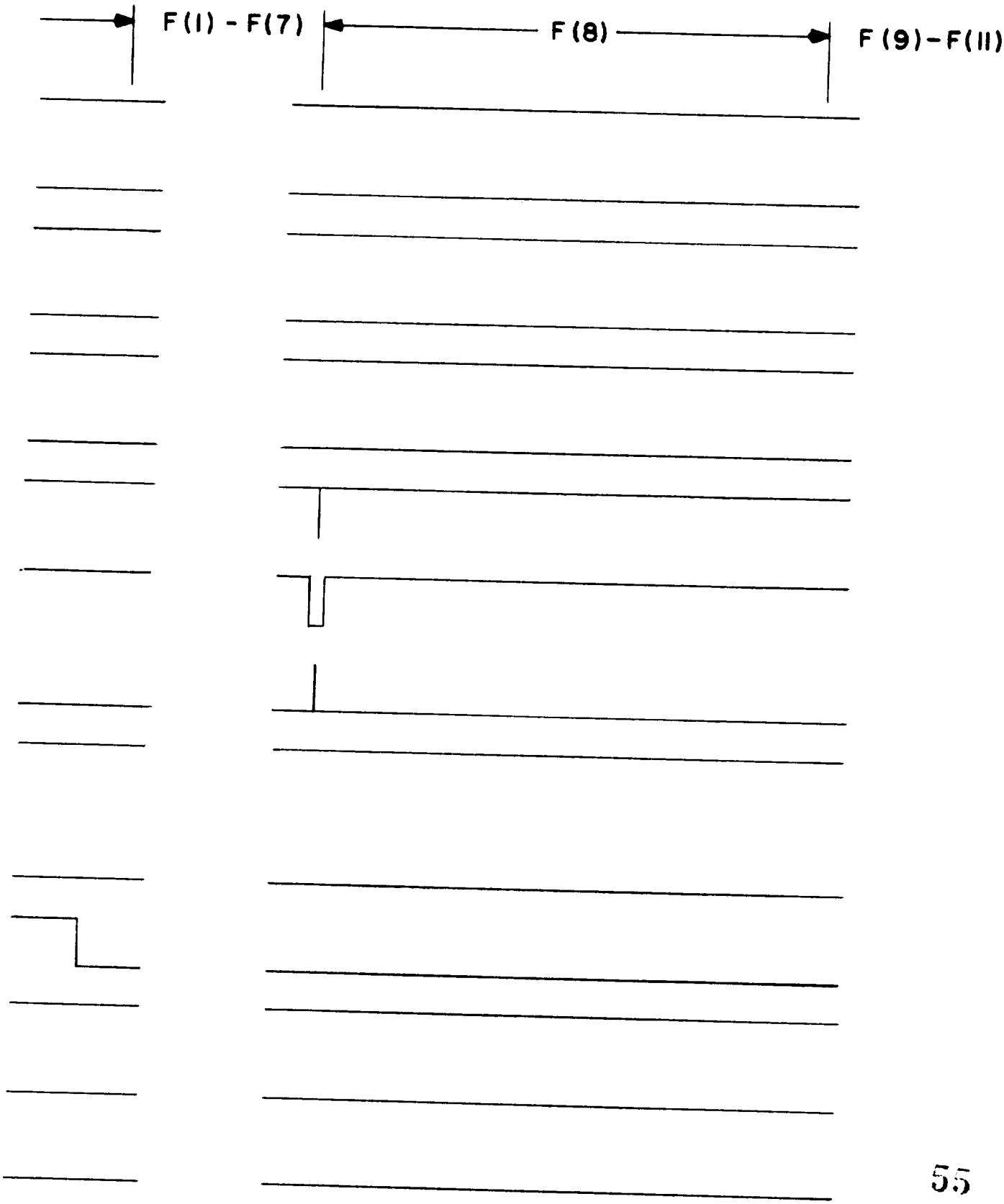
= L.S. PROGRAMMER


II-19-17
NORMAL H.S. SEQ. COUNT
II-18-31
II-18-34
II-19-13
MISSING SEQ.COUNT CORRECTION
II-18-31
II-18-34
II-19-10
II-19-12
II-19-13
ANG. CHAN. SEQ. COUNT
II-19-21
III-8-22
III-8-29
III-19-17
III-19-10
III-19-6

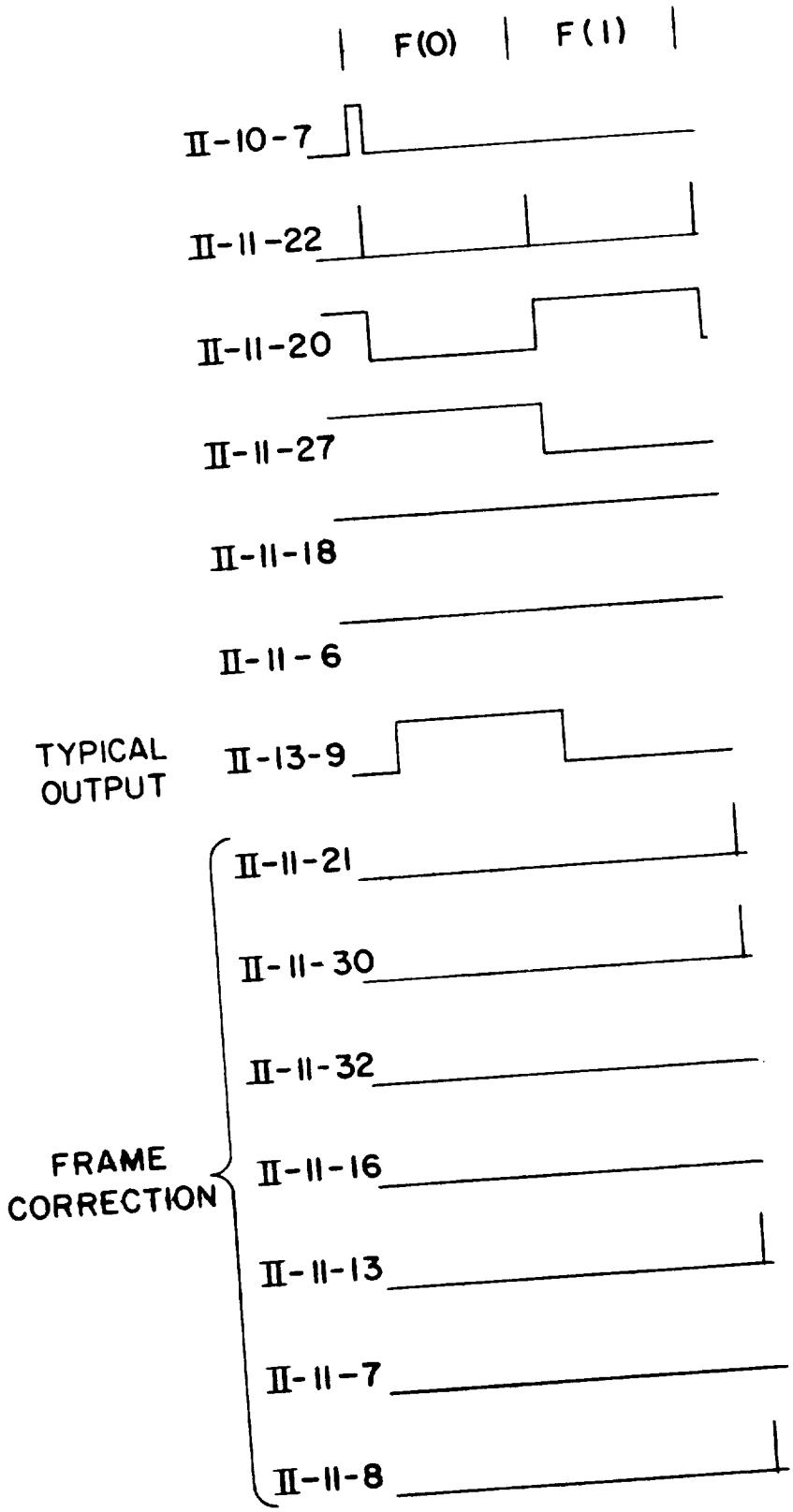
SEQUENCE COUNTER CONTROL TIMING (



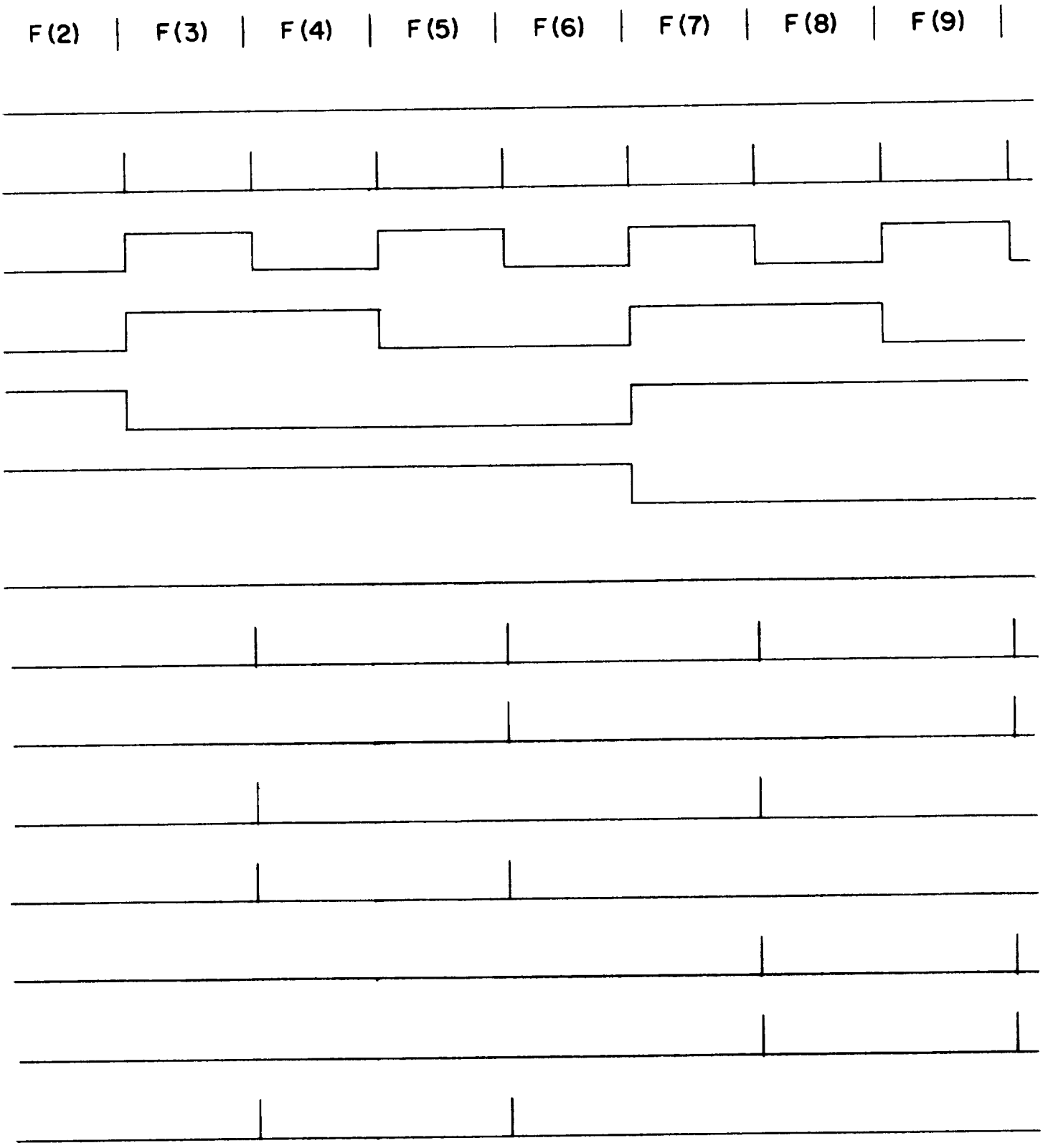
H.S. SEQUENCE)



S-51 FIGURE 25


F(0)
F(1)
II-10-7
II-11-22
II-11-20
II-11-27
II-11-18
II-11-6
TYPICAL OUTPUT
II-13-9
II-11-21
II-11-30
II-11-32
FRAME CORRECTION
II-11-16
II-11-13
II-11-7
II-11-8

H. S. FRAME SORTER TIM



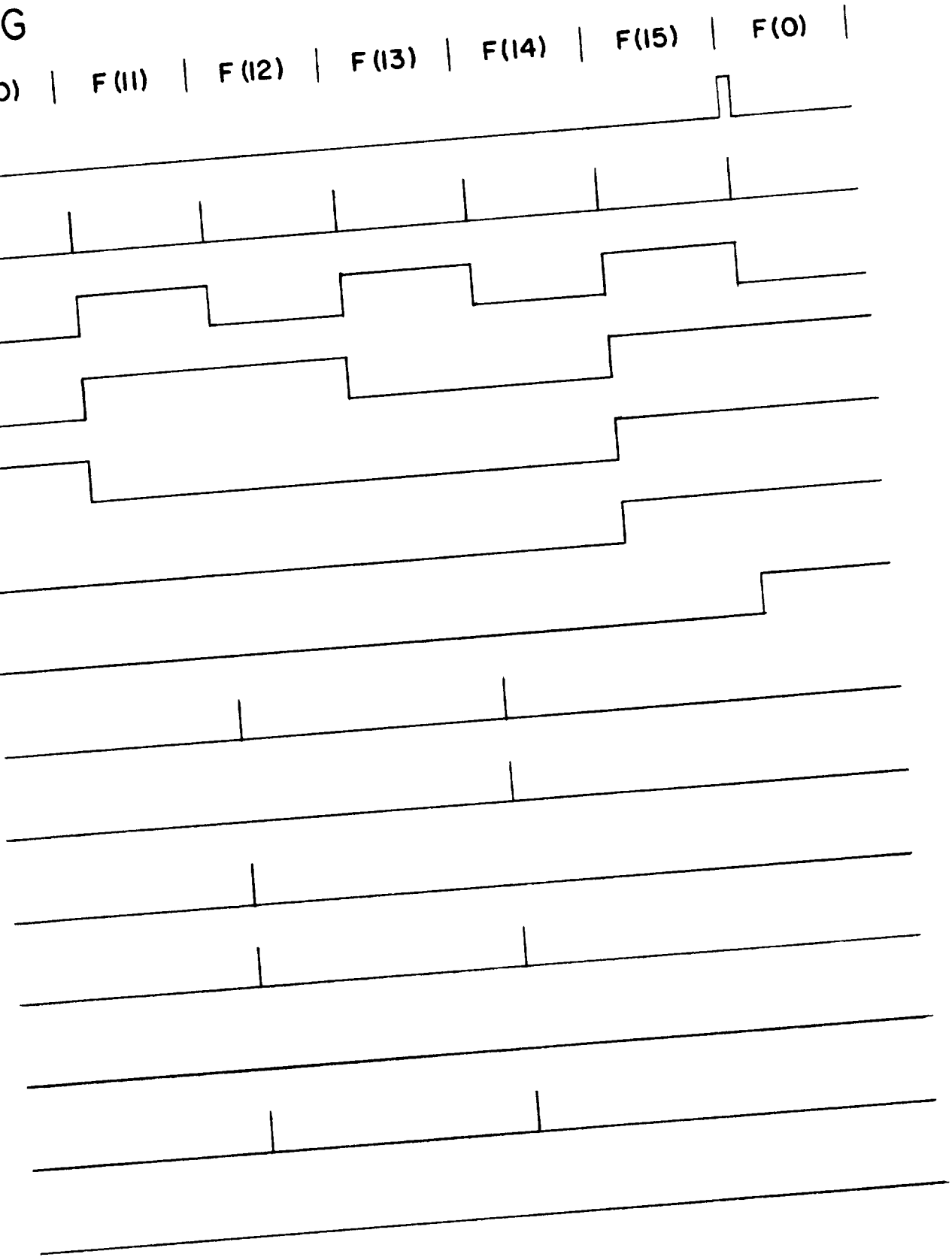
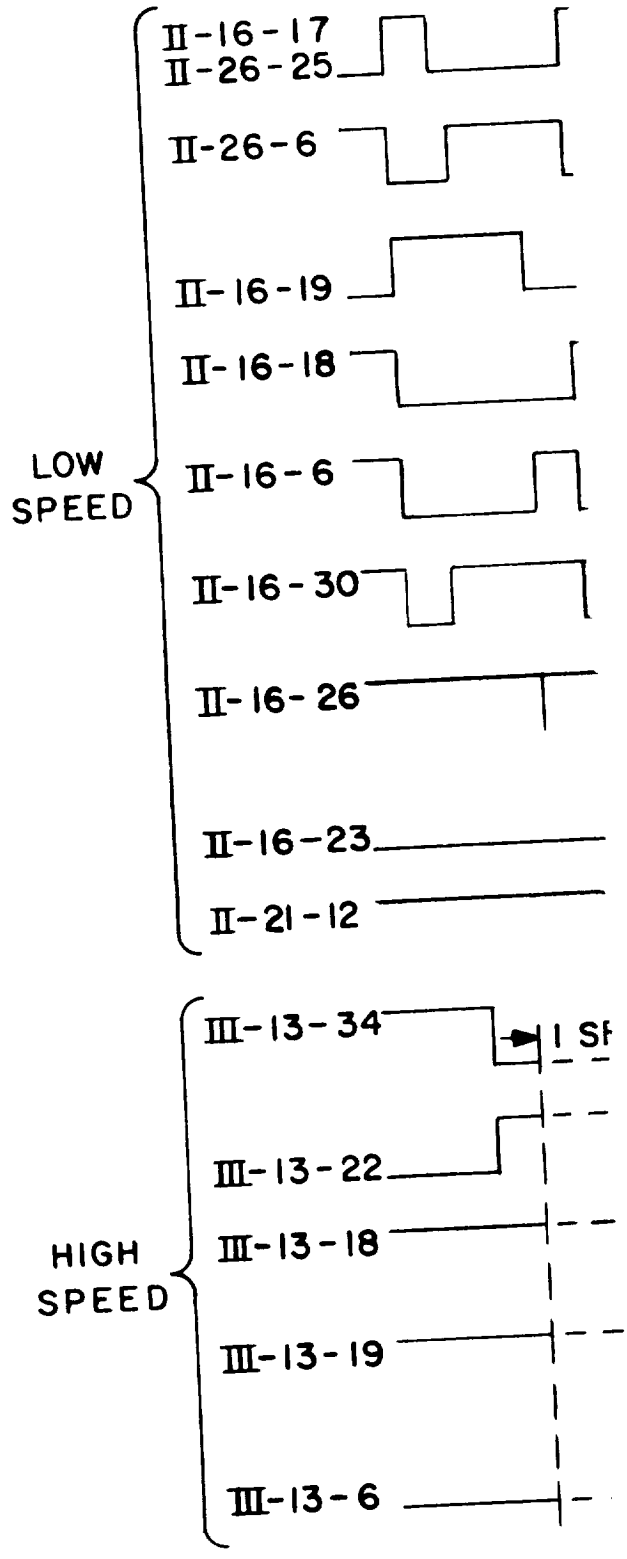
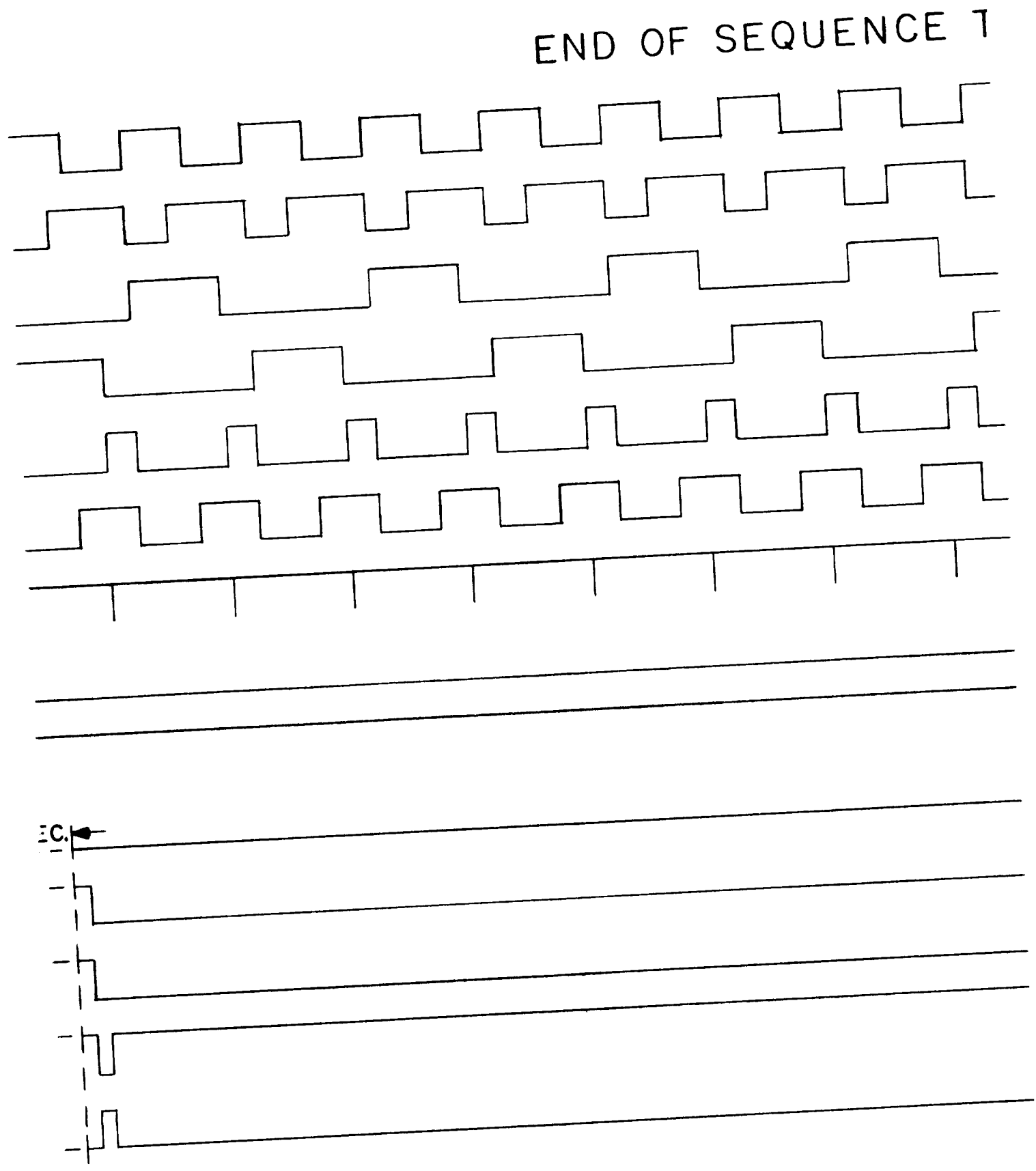
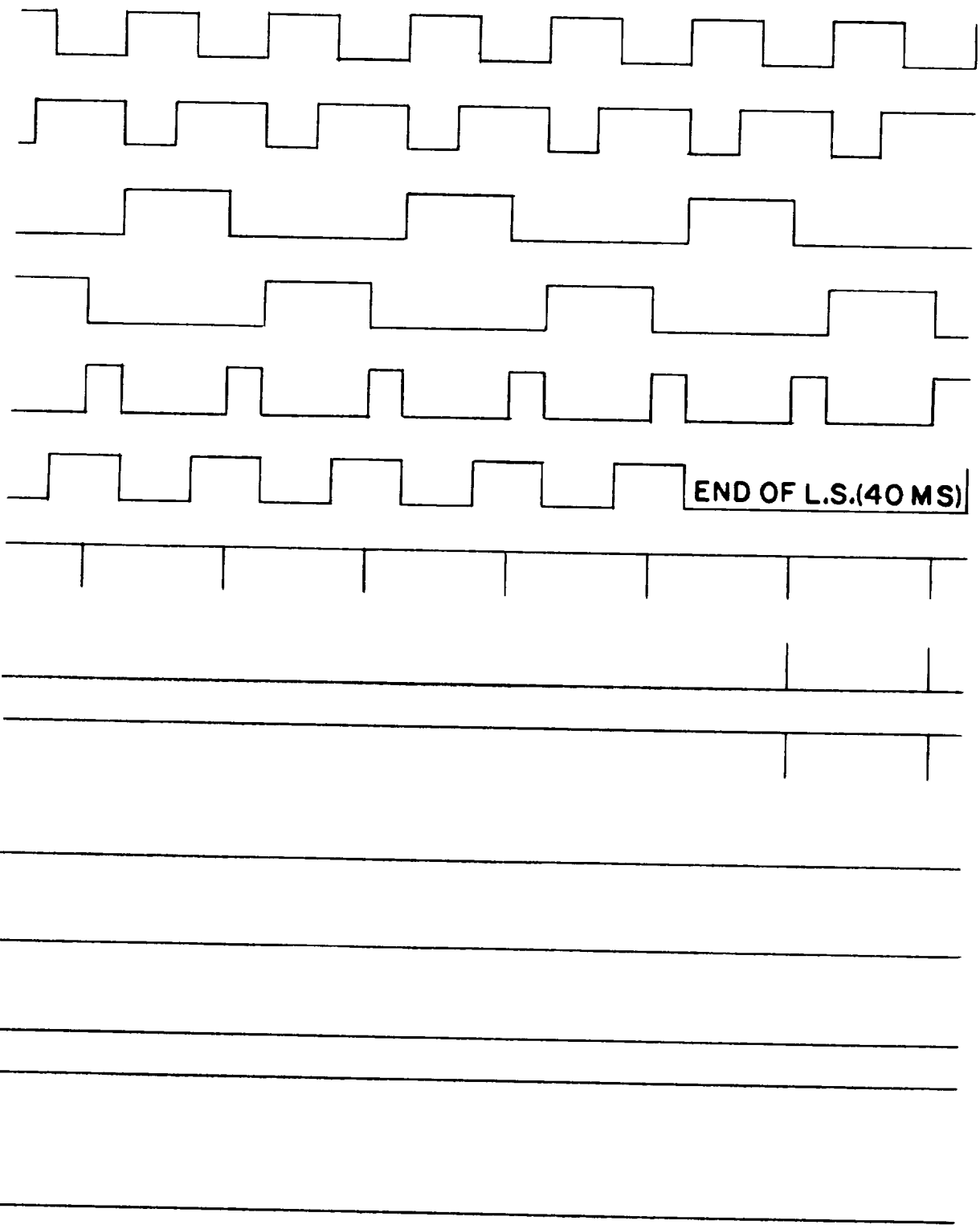


FIGURE 26

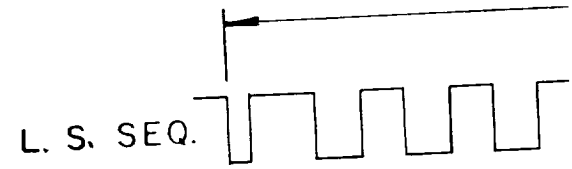

LOW SPEED
II-16-17
II-26-25
II-26-6
II-16-19
II-16-18
II-16-6
II-16-30
II-16-26
II-16-23
II-21-12
HIGH SPEED
III-13-34
III-13-22
III-13-18
III-13-19
III-13-6


END OF SEQUENCE T
EC.

TIMING



S-51 FIGURE 27



I-8-12
I-8-6
REGISTER RESET

REGISTER LOADING AND READOUT

I-2-27
I-2-18
FOR THE CASE WHE

I-3-20
I-3-27
FOR THE CASE WHE

COUNTER-REGISTER CLOCK INPUT CONTROL

I-8-29

I-11-25

III-18-34

I-2-22

I-2-20

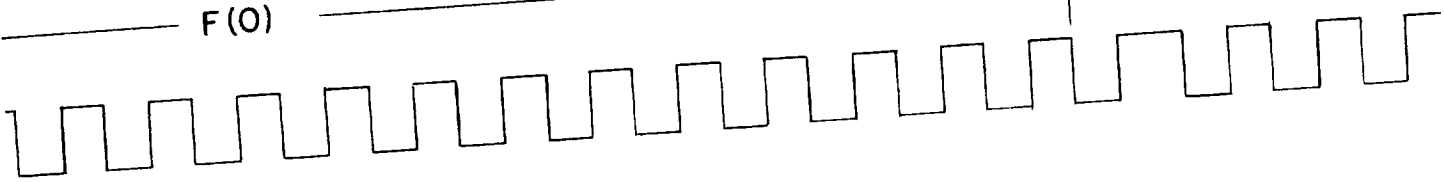
I-3-27

I-9-9

I-14-16

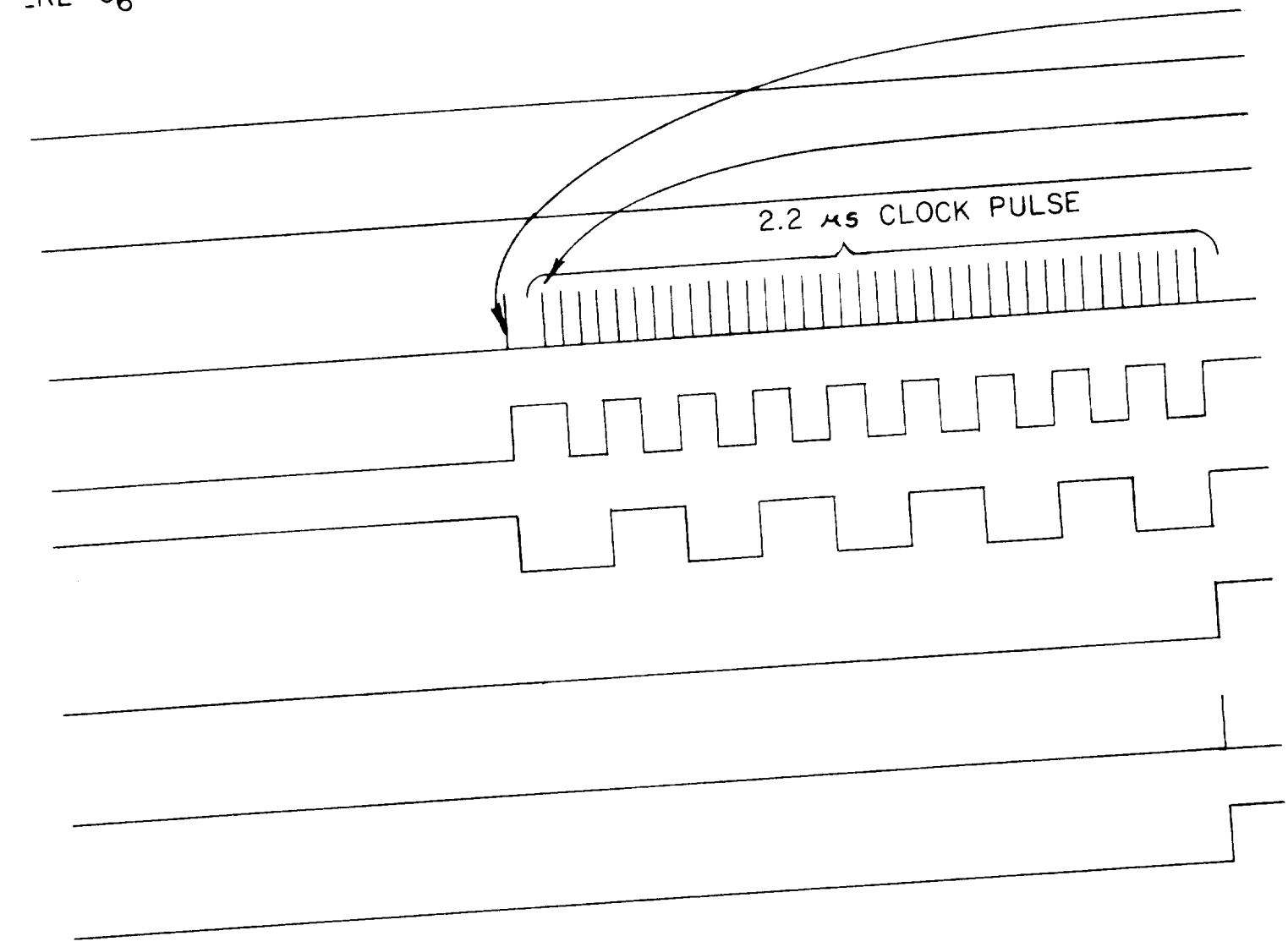
REGISTER TIMING (L. S. $C_{5,6}$ READOUT AS TYPICA

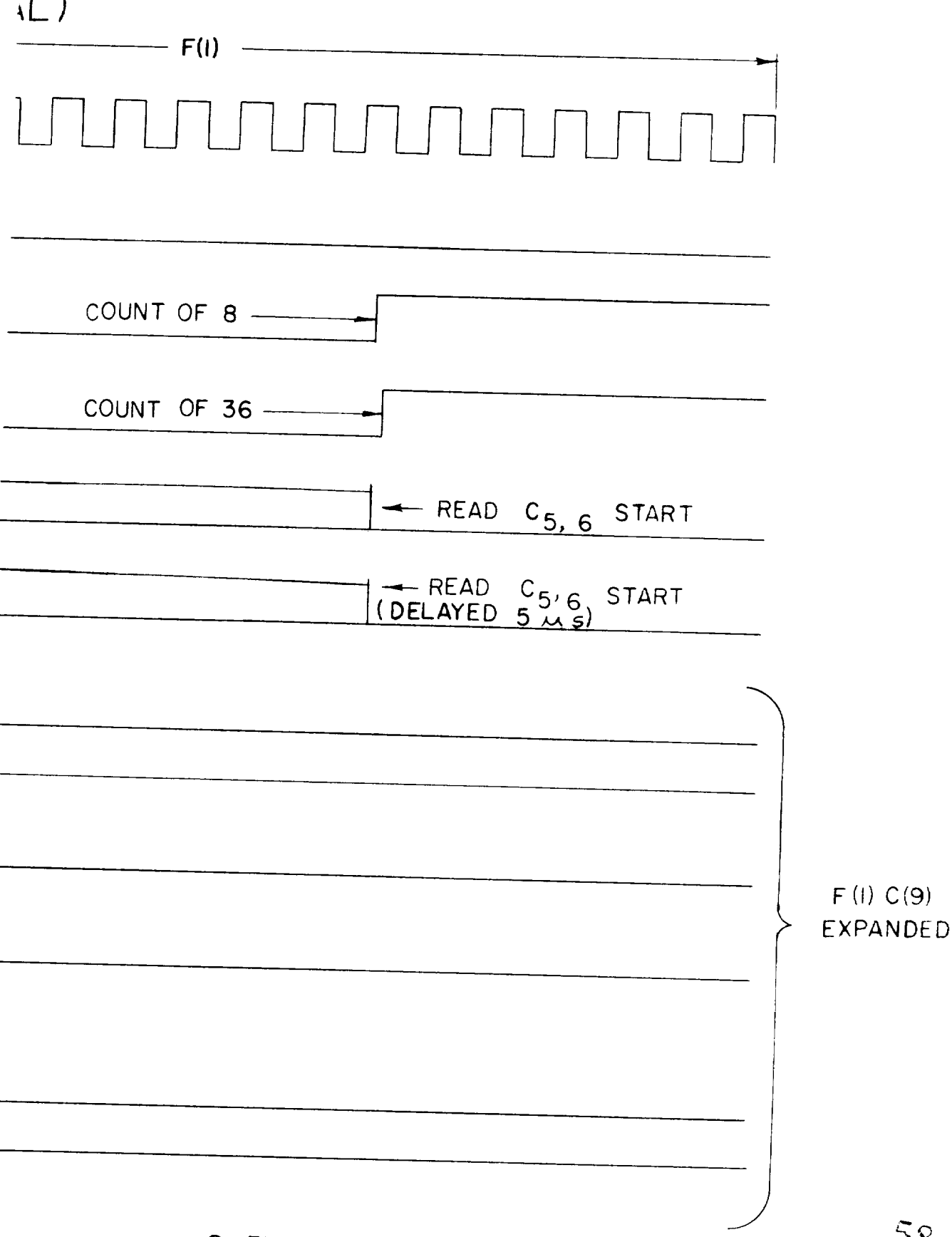
F(0)



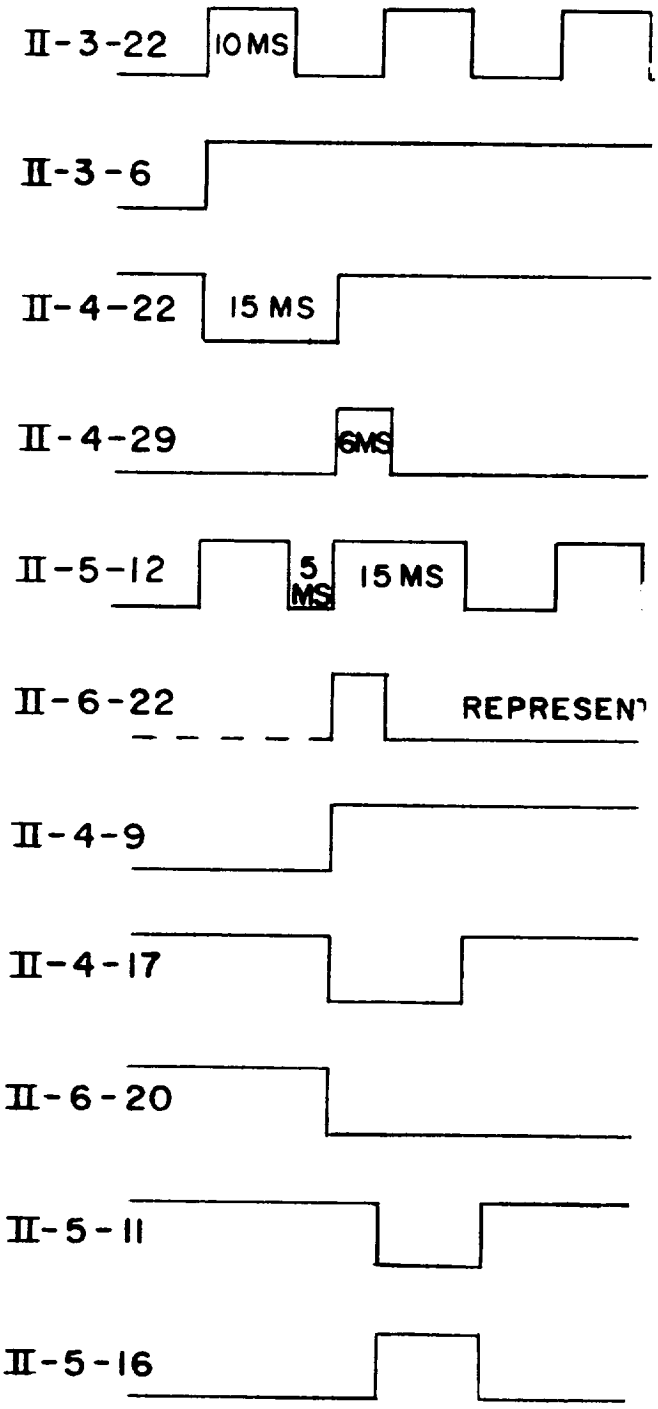
RE $C_5 \equiv 2^2=0;\ 2^1=0;\ 2^0=1$

ERE $C_6 \equiv 2^2=0;\ 2^1=0;\ 2^0=1$

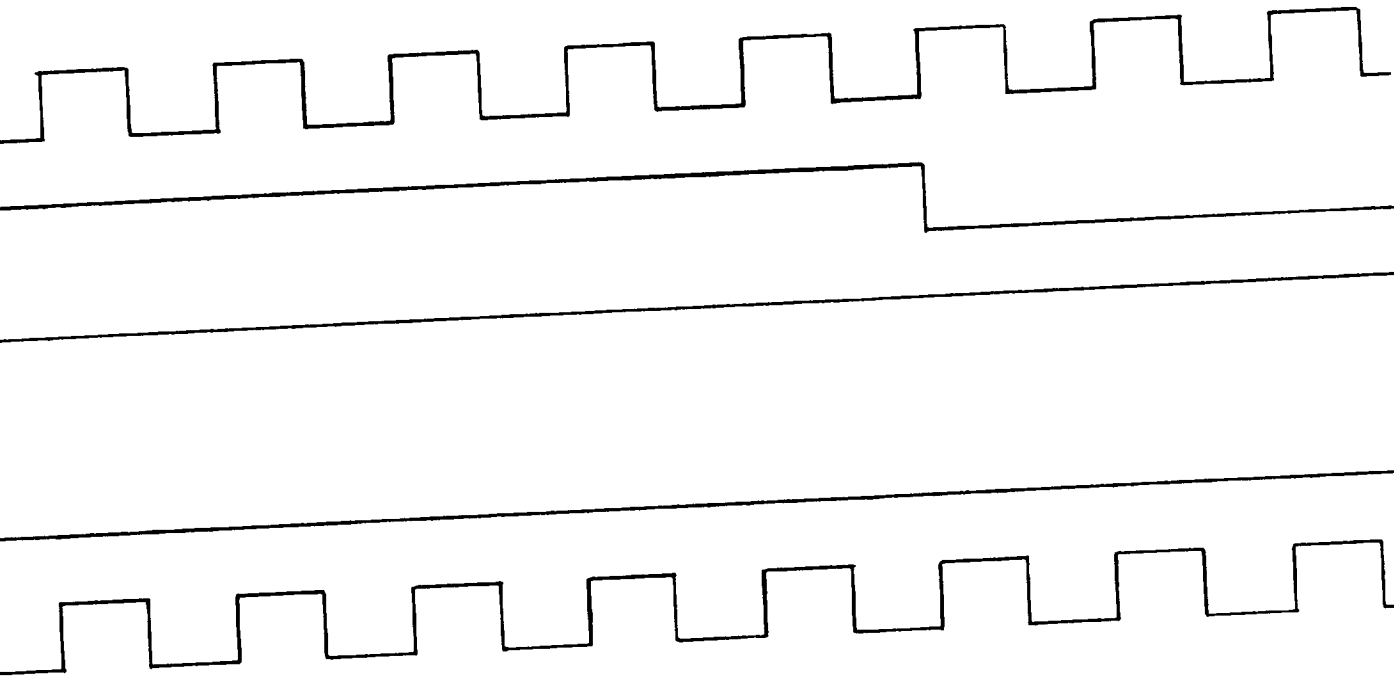




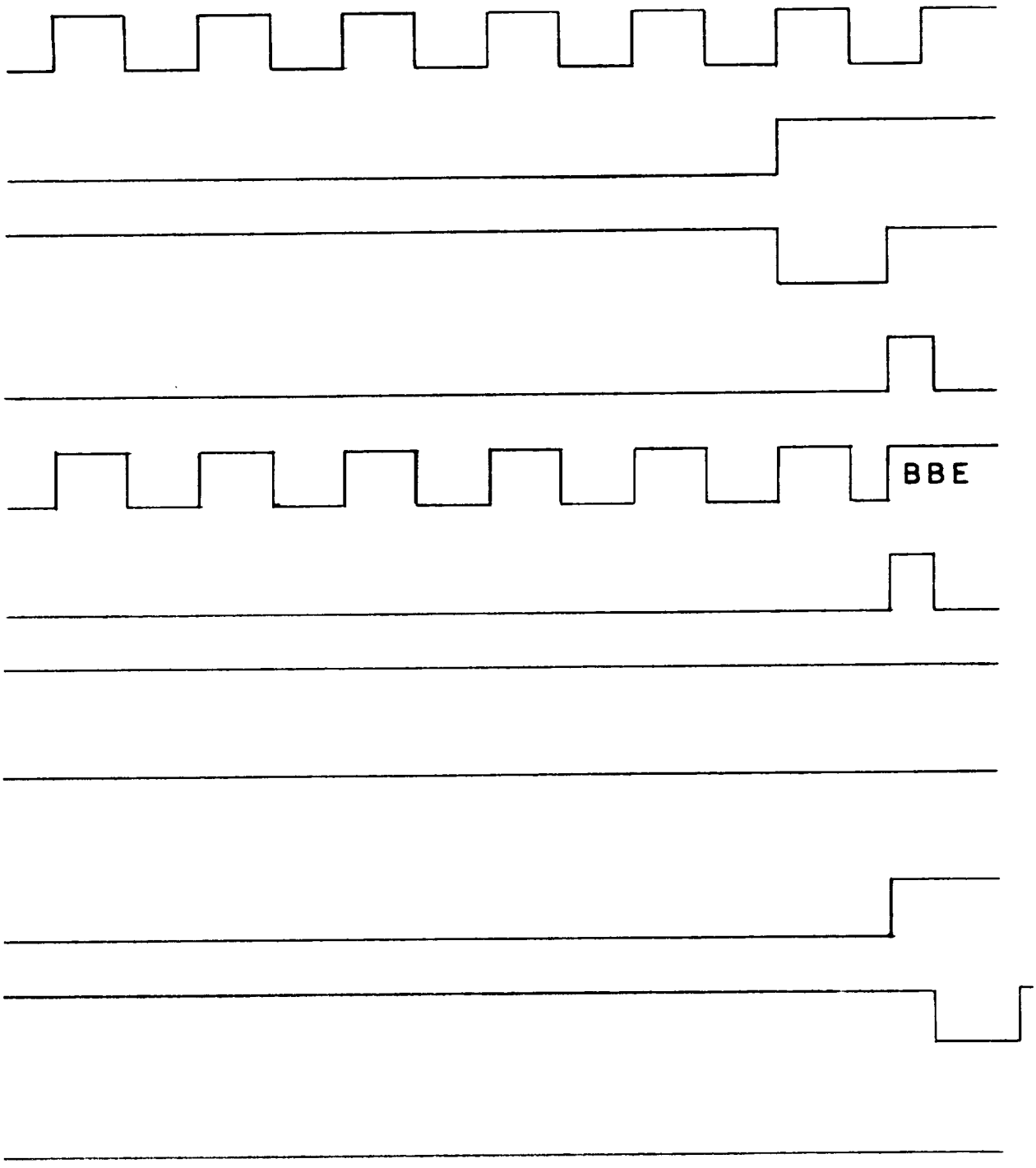
S-51 FIGURE 28


II-3-22
10MS
II-3-6
II-4-22
15 MS
II-4-29
6MS
II-5-12
5 MS
15 MS
II-6-22
REPRESEN
II-4-9
II-4-17
II-6-20
II-5-11
II-5-16

SIMULATOR TIMING



S 16TH OCCURRENCE



S-51 FIGURE 29

COMB-FILTER OUTPUT			H.S. TEST			L.S. TEST	
2^2	2^1	2^0	$C_{5,6}$	C_{1-4}	X	$C_{5,6}$	C_{1-4}
0	0	0	0	0	0	0	0
1	0	0	36	1168	18724	144	2336
0	1	0	18	4680	9362	72	9360
1	1	0	54	5848	28086	216	11696
0	0	1	9	2340	4681	36	4680
1	0	1	45	3508	23405	180	7016
0	1	1	27	7020	14043	108	14040
1	1	1	63	8188	32767	252	16376

DIGITAL COUNTER DISPLAY FOR TEST MODE

S-51 FIGURE 30

BL

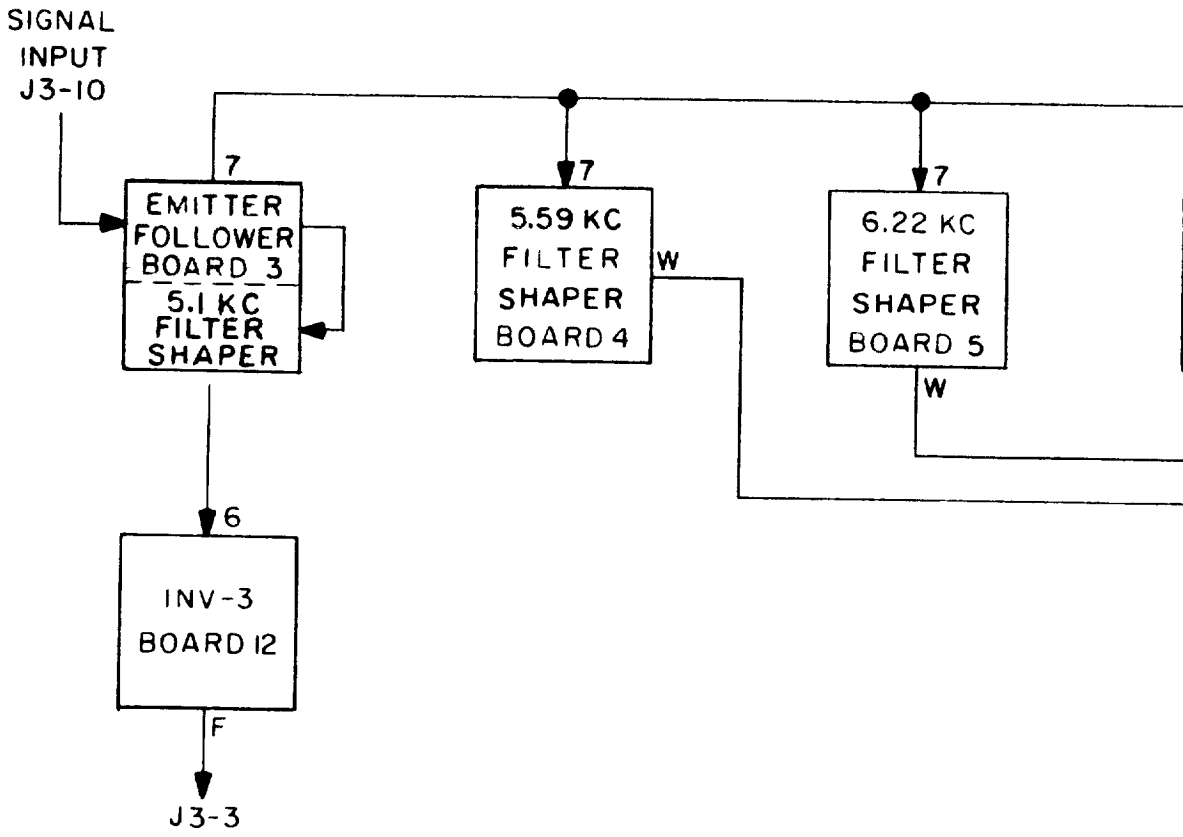

SIGNAL
INPUT
J3-10
7
EMITTER
FOLLOWER
BOARD 3
5.1 KC
FILTER
SHAPER
7
5.59 KC
FILTER
SHAPER
BOARD 4
W
7
6.22 KC
FILTER
SHAPER
BOARD 5
W
6
INV-3
BOARD 12
F
J3-3

DIAGRAM S-51 COMB FILTER

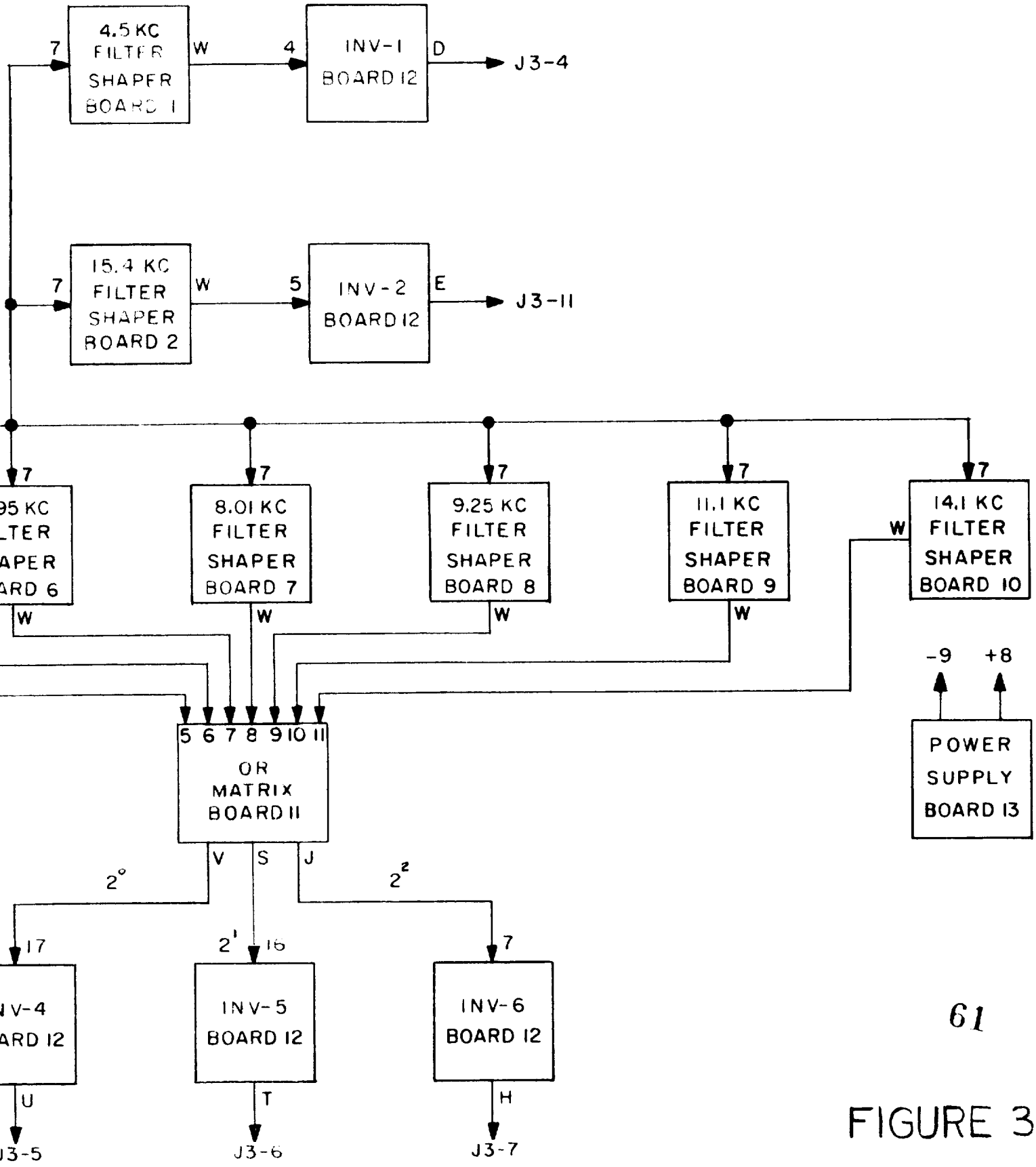
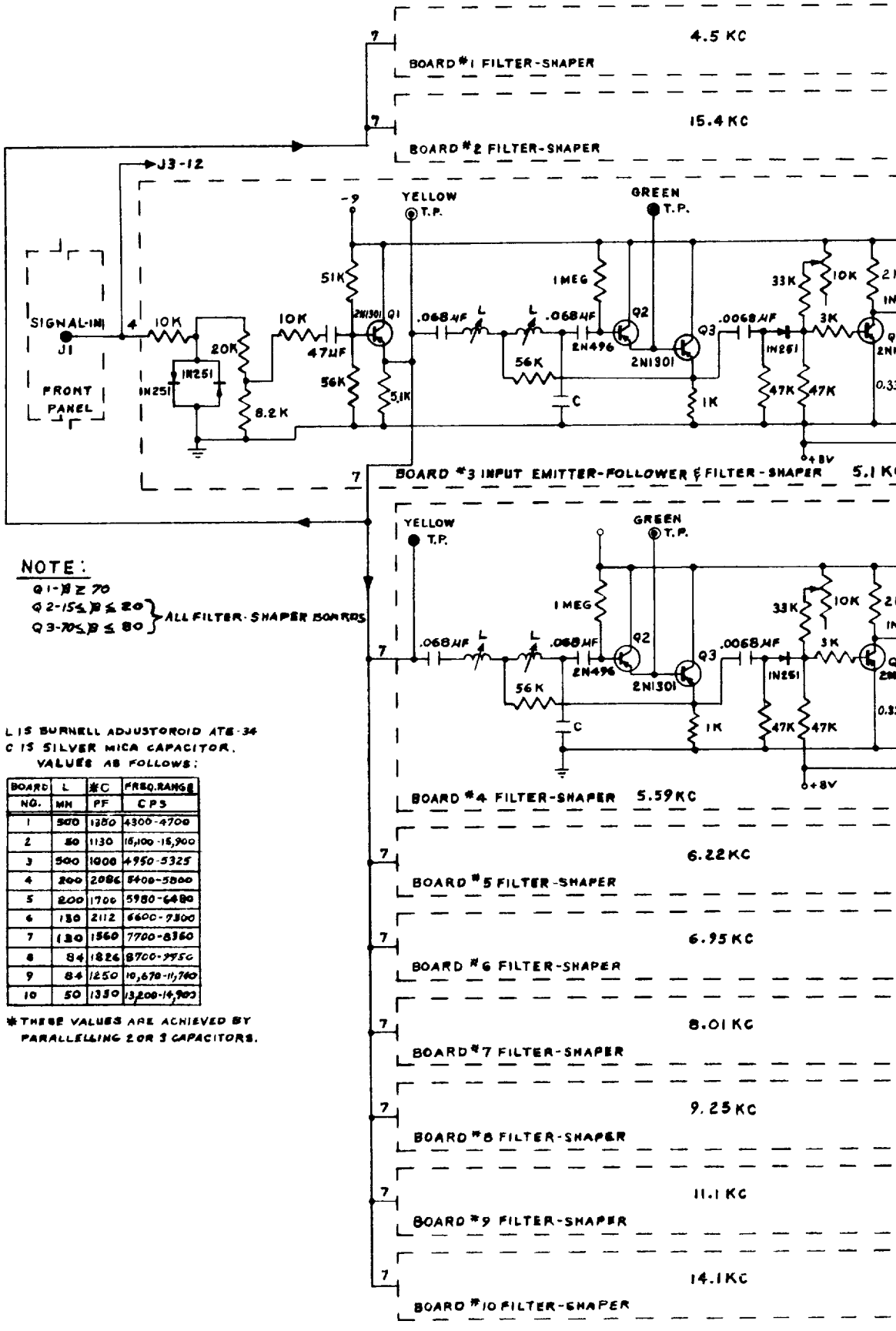


FIGURE 31



NOTE:

Q1-$\beta \geq 70$

Q2-$15 \leq \beta \leq 20$

Q3-$70 \leq \beta \leq 80$

} ALL FILTER-SHAPER BOARDS

L IS BURNELL ADJUSTOROID ATE-34

C IS SILVER MICA CAPACITOR.
VALUES AS FOLLOWS:

BOARD NO.	L MH	*C PF	FREQ. RANGE CPS
1	500	1350	4300-4700
2	50	1130	16,100-15,900
3	500	1000	4950-5325
4	200	2086	5400-5800
5	200	1700	5980-6480
6	130	2112	6600-7300
7	130	1560	7700-8360
8	84	1826	8700-9550
9	84	1250	10,670-11,760
10	50	1350	13,200-14,900

*THESE VALUES ARE ACHIEVED BY PARALLELLING 2 OR 3 CAPACITORS.

S-51 TEST STAND COMB FILTER

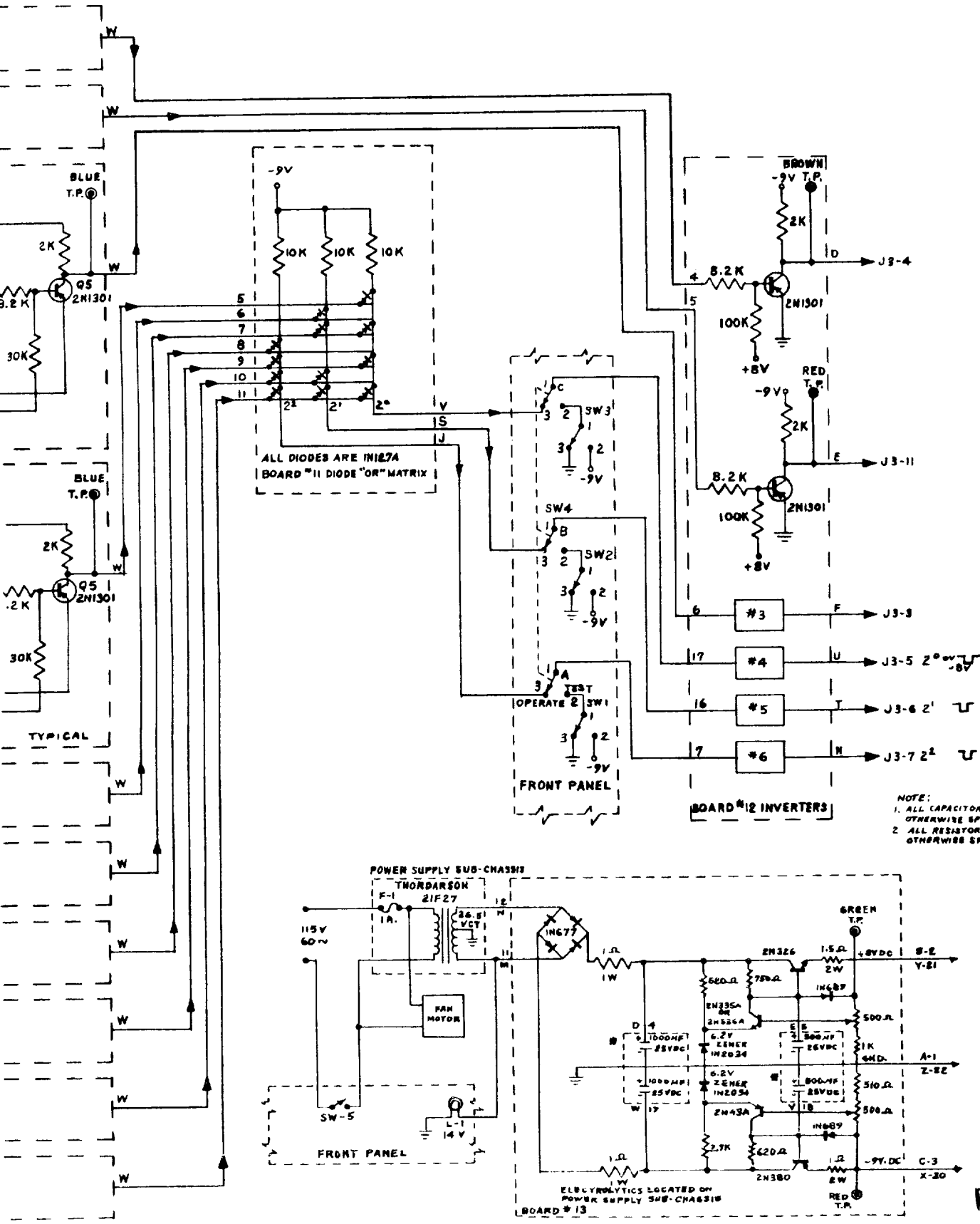
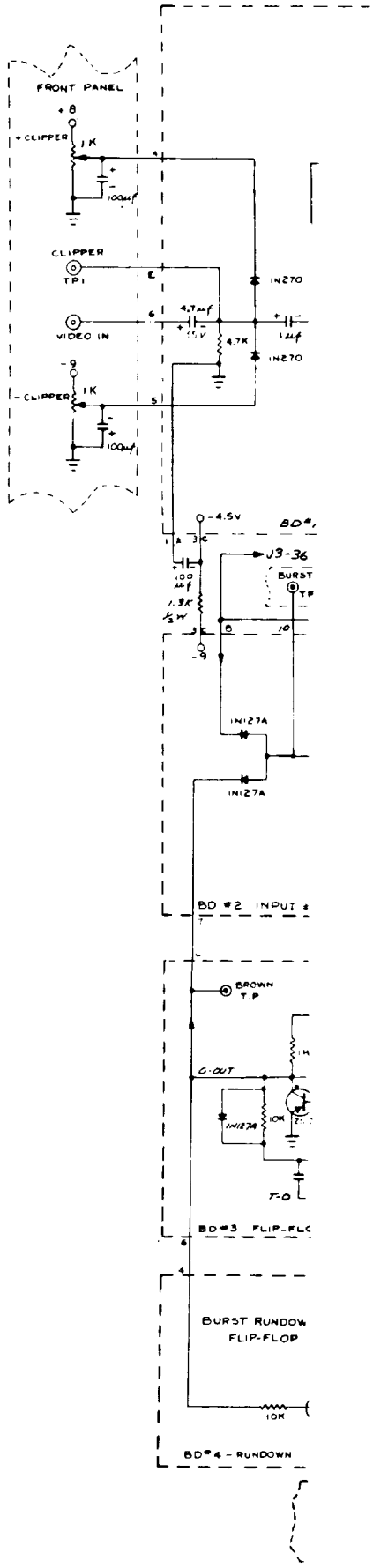
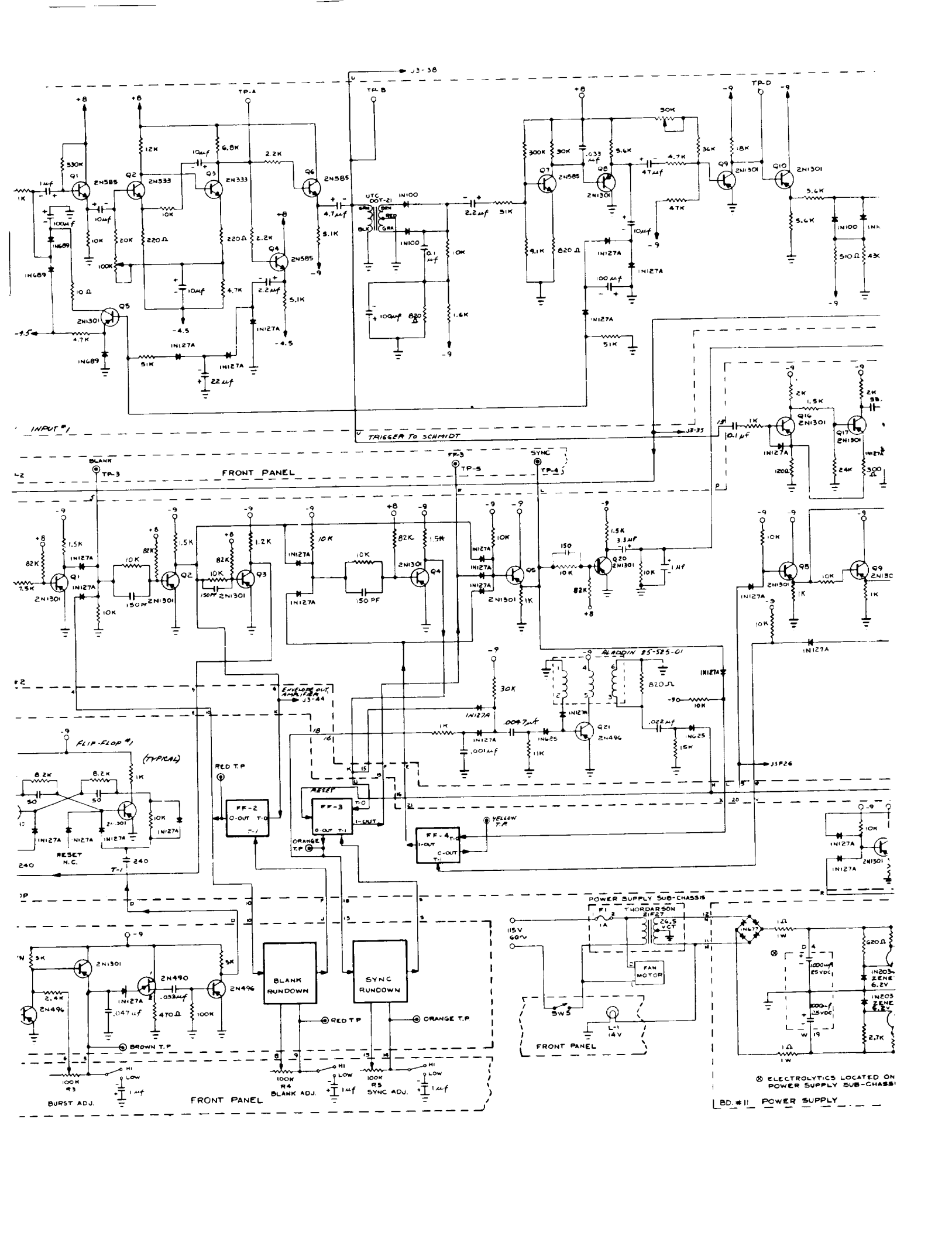
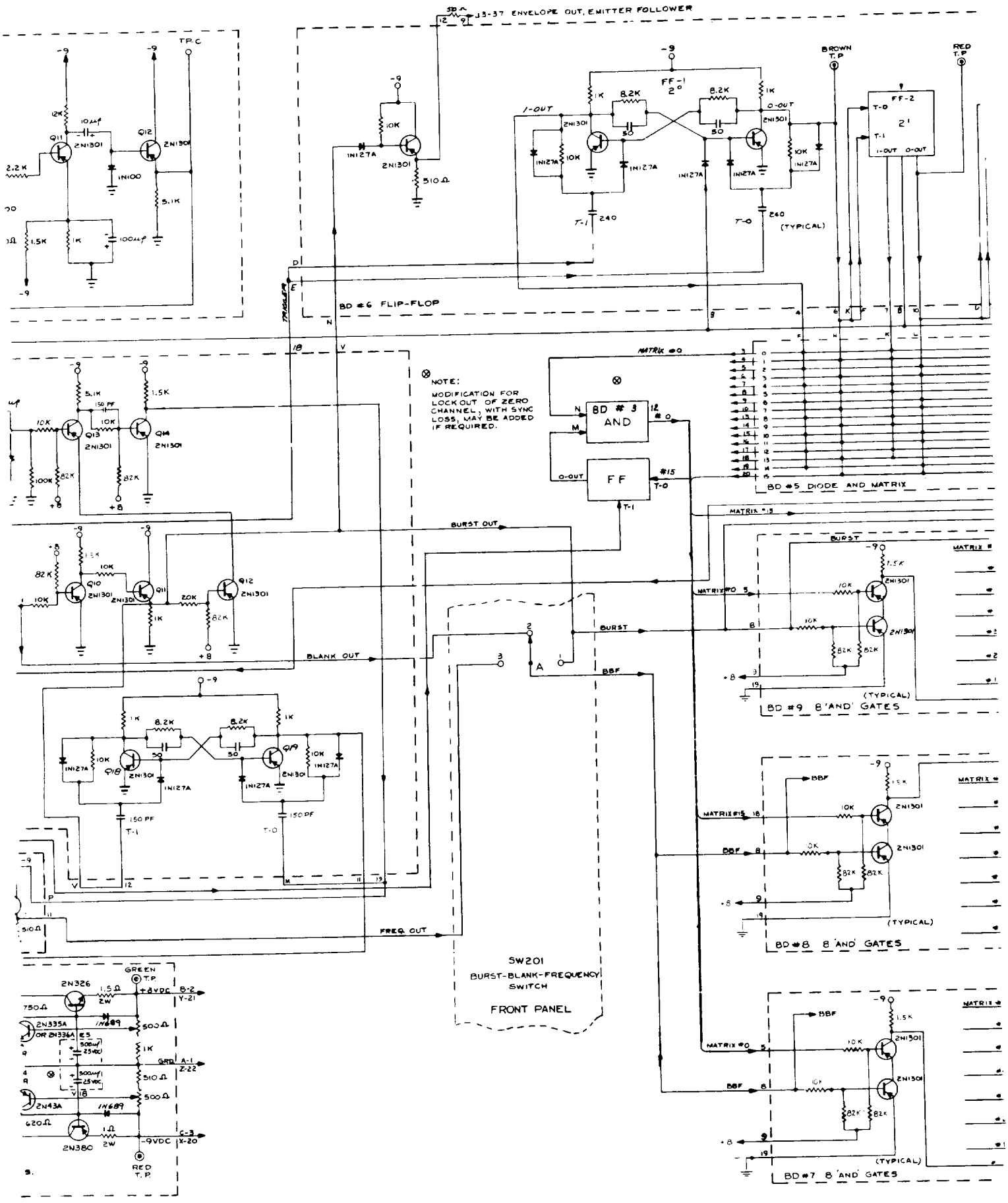
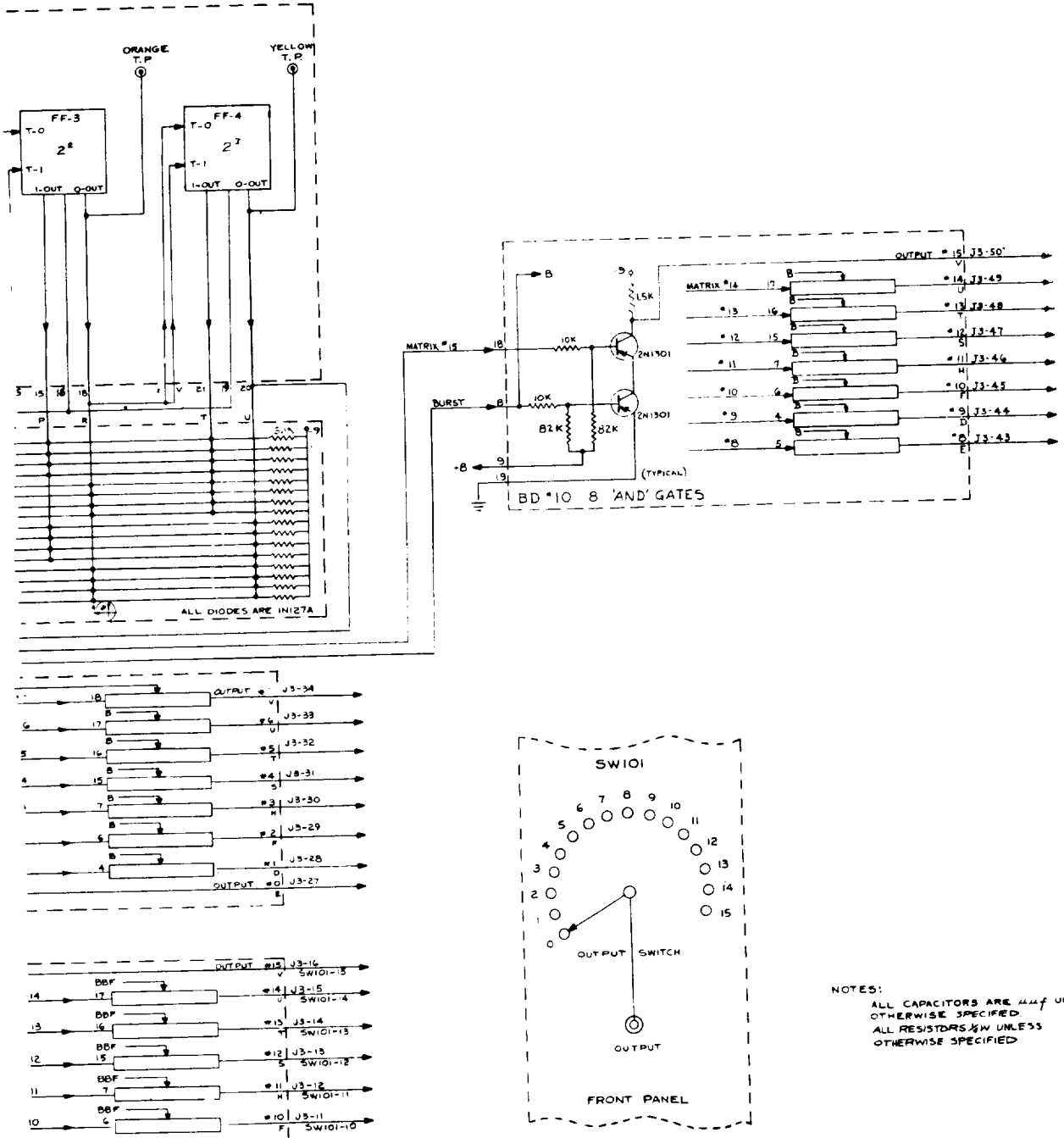


FIGURE 32


FRONT PANEL
+8
+ CLIPPER
1K
100μf
CLIPPER
TP1
VIDEO IN
- CLIPPER
1K
100μf
IN270
4.7μf
15V
4.7K
1μf
IN270
-4.5V
BD#
J3-36
100 μf
1.3K
½W
BURST
TP
IN127A
IN127A
BD #2 INPUT
BROWN
T P
C-OUT
1K
10K
IN127A
T-O
BD#3 FLIP-FLO
BURST RUNDOWN
FLIP-FLOP
10K
BD#4 - RUNDOWN


INPUT #1
TRIGGER TO SCHMIDT
FRONT PANEL
FLIP-FLOP #1 (TYPICAL)
RESET N.C.
RED T.P
ORANGE T.P
YELLOW T.P
BROWN T.P
BLANK RUNDOWN
SYNC RUNDOWN
BURST ADJ.
BLANK ADJ.
SYNC ADJ.
POWER SUPPLY SUB-CHASSIS
115V 60~
FAN MOTOR
BD. #11 POWER SUPPLY
⊗ ELECTROLYTICS LOCATED ON POWER SUPPLY SUB-CHASSIS


J3-37 ENVELOPE OUT, EMITTER FOLLOWER
BD #6 FLIP-FLOP
FF-1
FF-2
BROWN T.P
RED T.P
NOTE:
MODIFICATION FOR LOCK OUT OF ZERO CHANNEL; WITH SYNC LOSS, MAY BE ADDED IF REQUIRED.
BD # 5 AND
FF
BD #5 DIODE AND MATRIX
BURST OUT
BLANK OUT
FREQ OUT
BURST
BBF
SW201
BURST-BLANK-FREQUENCY SWITCH
FRONT PANEL
BD #9 8 'AND' GATES
BD #8 8 'AND' GATES
BD #7 8 'AND' GATES
(TYPICAL)
GREEN T.P
RED T.P
+8VDC
-9VDC



NOTES:
ALL CAPACITORS ARE μμf UNLESS OTHERWISE SPECIFIED.
ALL RESISTORS ½W UNLESS OTHERWISE SPECIFIED

FIGURE 33